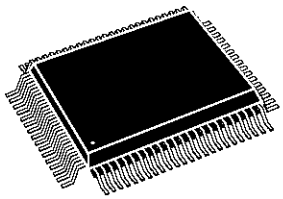
SGS-THOMSON MICROELECTRONICS

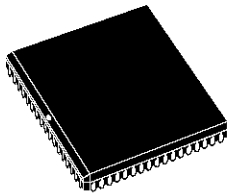
ST9040

16K ROM HCMOS MCU WITH EEPROM, RAM AND A/D CONVERTER

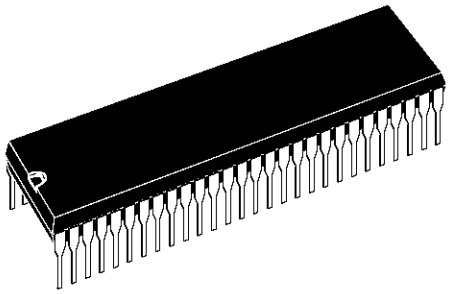
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time : 500ns (12MHz internal)
- Internal Memory :
  ROM 16K bytes
  RAM 256 bytes
  EEPROM 512 bytes
  224 general purpose registers available as RAM, accumulators or index registers (register file)
- 80-pin PQFP package for ST9040Q
- 68-lead PLCC package for ST9040C
- 56-pin shrink DIP package for ST9040B
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- Up to 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Windowed and One Time Programmable EPROM parts available for prototyping and pre-production development phases
- Pin to pin compatible with ST9030 and ST9036



PQFP80



PLCC68



PSDIP56

(Ordering Information at the end of the Datasheet)

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Figure 1. 80 Pin PQFP Package

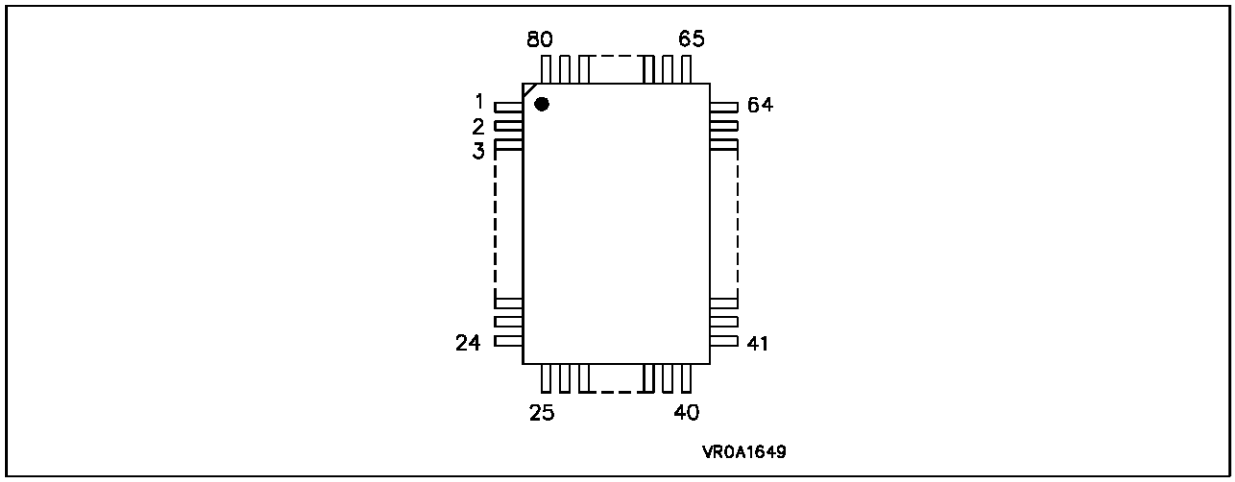


Table 1. ST9040Q Pin Description

Pin	Name
1	AV_{SS}
2	AV_{SS}
3	NC
4	P44/AIN4
5	P57
6	P56
7	P55
8	P54
9	INT7
10	INT0
11	P53
12	NC
13	P52
14	P51
15	P50
16	OSCOUT
17	V_{SS}
18	V_{SS}
19	NC
20	OSCIN
21	$\overline{RESET}$
22	P37/T1OUTB
23	P36/T1INB
24	P35/T1OUTA

Pin	Name
25	P34/T1INA
26	P33/T0OUTB
27	P32/T0INB
28	P31/T0OUTA
29	P30/P/$\overline{D}$/T0INA
30	A15
31	A14
32	NC
33	A13
34	A12
35	A11
36	A10
37	A9
38	A8
39	P00/A0/D0
40	P01/A1/D1

Pin	Name
64	P20/NMI
63	NC
62	V_{SS}
61	P70/SIN
60	P71/SOUT
59	P72/INT4/TXCLK /CLKOUT
58	P73/INT5 /RXCLK/ADTRG
57	P74/P/$\overline{D}$/INT6
56	P75/$\overline{WAIT}$
55	P76/$\overline{WDOUT}$ /$\overline{BUSREQ}$
54	P77/WDIN /$\overline{BUSACK}$
53	R/$\overline{W}$
52	NC
51	$\overline{DS}$
50	$\overline{AS}$
49	NC
48	V_{DD}
47	V_{DD}
46	P07/A7/D7
45	P06/A6/D6
44	P05/A5/D5
43	P04/A4/D4
42	P03/A3/D3
41	P02/A2/D2

Pin	Name
80	AV_{DD}
79	NC
78	P47/AIN7
77	P46/AIN6
76	P45/AIN5
75	P43/AIN3
74	P42/AIN2
73	P41/AIN1
72	P40/AIN0
71	P27/RRDY5
70	P26/INT3 /$\overline{RDSTB5}$/P/$\overline{D}$
69	P25/WRRDY5
68	P24/INT1 /$\overline{WRSTB5}$
67	P23/SDO
66	P22/INT2/SCK
65	P21/SDI/P/$\overline{D}$

Figure 2. 68 Pin PLCC Package

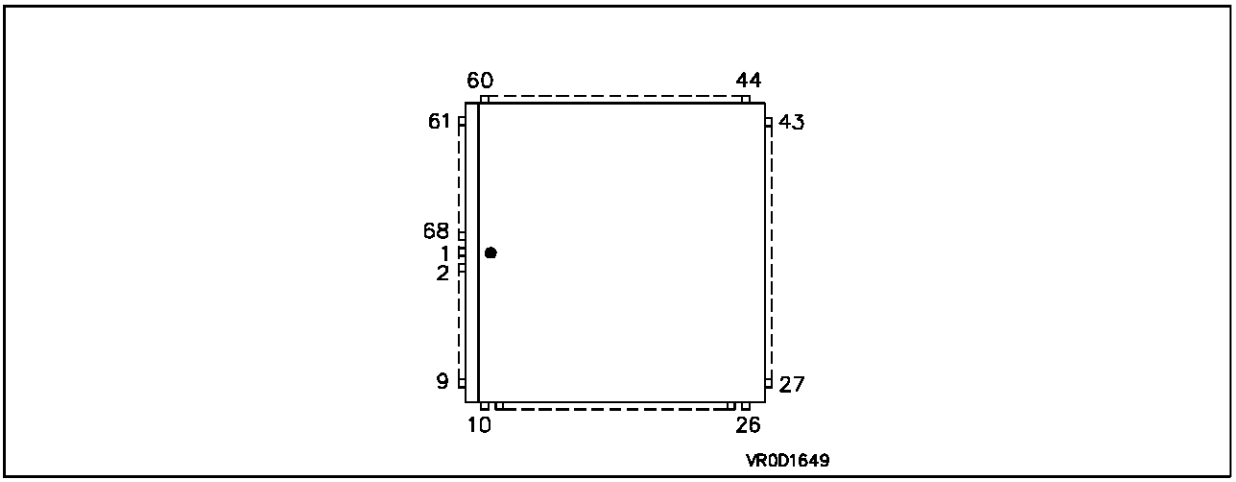


Table 2. ST9040C Pin Description

Pin	Name
61	P44/AIN4
62	P57
63	P56
64	P55
65	P54
66	INT7
67	INT0
68	P53
● 1	P52
2	P51
3	P50
4	OSCOUT
5	V_{SS}
6	OSCIN
7	$\overline{\text{RESET}}$
8	P37/T1OUTB
9	P36/T1INB

Pin	Name
10	P35/T1OUTA
11	P34/T1INA
12	P33/T0OUTB
13	P32/T0INB
14	P31/T0OUTA
15	P30/P/$\overline{\text{D}}$/T0INA
16	P17/A15
17	P16/A14
18	P15/A13
19	P14/A12
20	P13/A11
21	P12/A10
22	P11/A9
23	P10/A8
24	P00/A0/D0
25	P01/A1/D1
26	P02/A2/D2

Pin	Name
43	P70/SIN
42	P71/SOUT
41	P72/CLKOUT /TXCLK/INT4
40	P73/ADTRG /RXCLK/INT5
39	P74/P/$\overline{\text{D}}$/INT6
38	$\overline{\text{P75/WAIT}}$
37	P76/WDOUT /$\overline{\text{BUSREQ}}$
36	P77/WDIN /$\overline{\text{BUSACK}}$
35	R/$\overline{\text{W}}$
34	$\overline{\text{DS}}$
33	$\overline{\text{AS}}$
32	V_{DD}
31	P07/A7/D7
30	P06/A6/D6
29	P05/A5/D5
28	P04/A4/D4
27	P03/A3/D3

Pin	Name
60	AV_{SS}
59	AV_{DD}
58	P47/AIN7
57	P46/AIN6
56	P45/AIN5
55	P43/AIN3
54	P42/AIN2
53	P41/AIN1
52	P40/AIN0
51	P27/RRDY5
50	P26/INT3 /$\overline{\text{RDSTB}}$5/P/$\overline{\text{D}}$
49	P25/WRRDY5
48	P24/INT1 /$\overline{\text{WRSTB}}$5
47	P23/SDO
46	P22/INT2/SCK
45	P21/SDI/P/$\overline{\text{D}}$
44	P20/NMI

Figure 1b. 56 Pin Shrink DIP Pinout

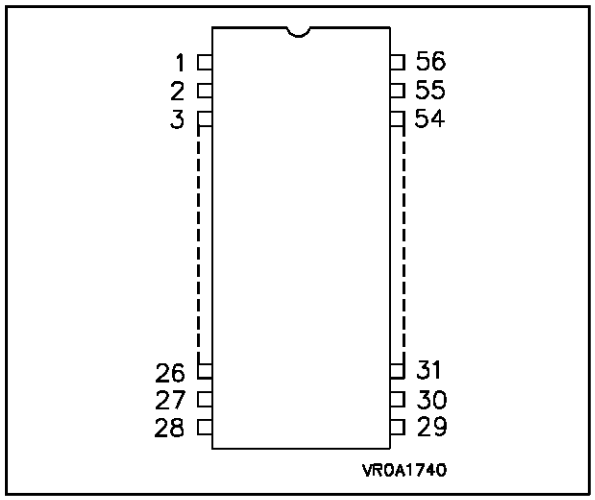


Table 3. ST9040B Pin Description

Pin	Pin name
1	P42/AIN2
2	P43/AIN3
3	P45/AIN5
4	P46/AIN6
5	P47/AIN7
6	AVDD
7	AVSS
8	P44/AIN4
9	P57
10	P56
11	P55
12	P54
13	P53
14	P52
15	OSCOUT
16	V_{SS}
17	OSCIN
18	$\overline{\text{RESET}}$
19	P37/T1OUTB
20	P36/T1INB
21	NC
22	P35/T1OUTA
23	P34/T1INA
24	P33/T0OUTB
25	P32/T0INB
26	P31/T0OUTA
27	P30/P/D/T0INA
28	P13/A11

Pin	Pin name
56	P41/AIN1
55	P40/AIN0
54	P23/SDO
53	P22/INT2/SCK
52	P21/SDI/P/$\overline{\text{D}}$
51	P20/NMI
50	P70/SIN
49	P71/SOUT
48	P72/CLKOUT TXCLK/INT4
47	P73/ADTRG RXCLK/INT5
46	P76WDOUT/$\overline{\text{BUSREQ}}$
45	P77/WDIN/BUSACK
44	R/$\overline{\text{W}}$
43	DS
42	$\overline{\text{AS}}$
41	V_{DD}
40	V_{SS}
39	P07/A7/D7
38	P06/A6/D6
37	P05/A5/D5
36	P04/A4/D4
35	P03/A3/D3
34	P02/A2/D2
33	P01/A1/D1
32	P00/A0/D0
31	P10/A8
30	P11/A9
29	P12/A10

1.1GENERAL DESCRIPTION

The ST9040 is a ROM member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ST9040 peripheral and functional actions are fully compatible throughout the ST903x/4x family. This datasheet will thus provide only information specific to this ROM device.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9030 ROM-BASED DEVICE FOR FURTHER DETAILS.

The nucleus of the ST9040 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set. The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST9040 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer. In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

1.2 PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

DS. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of **$\overline{DS}$**. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST9040 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

INT0, INT7. External interrupts (input, active on rising or falling edge). External interrupt inputs 0 and 7 respectively. INT0 channel may also be used for the timer watchdog interrupt.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter. *Must be tied to V_{SS}.*

V_{DD}. Main Power Supply Voltage (5V ± 10%)

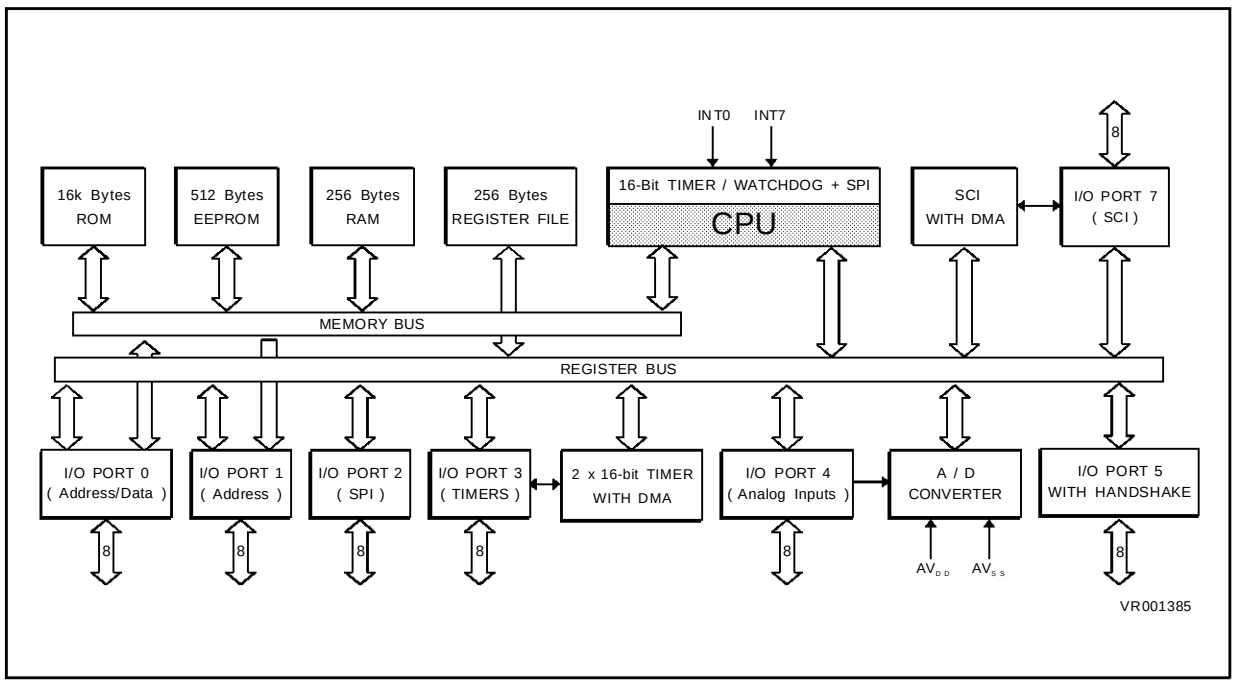
V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible)*. 56 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as alternate functions.

1.2.1 I/O Port Alternate Functions

Each pin of the I/O ports of the ST9040 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1-4 shows the Functions allocated to each I/O Port pins and a summary of packages for which they are available.

Figure 3. ST9040 Block Diagram



PIN DESCRIPTION (Continued)

Table 4. ST9040 I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
Port. bit				PLCC	PQFP	PSDIP
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24	39	32
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25	40	33
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26	41	34
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27	42	35
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28	43	36
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29	44	37
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30	45	38
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31	46	39
P1.0	A8	O	Address bit 8	23	38	31
P1.1	A9	O	Address bit 9	22	37	30
P1.2	A10	O	Address bit 10	21	36	29
P1.3	A11	O	Address bit 11	20	35	28
P1.4	A12	O	Address bit 12	19	34	
P1.5	A13	O	Address bit 13	18	33	
P1.6	A14	O	Address bit 14	17	31	
P1.7	A15	O	Address bit 15	16	30	
P2.0	NMI	I	Non-Maskable Interrupt	44	64	51
P2.0	ROMless	I	ROMless Select (Mask option)	44	64	51
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45	65	
P2.1	SDI	I	SPI Serial Data Out	45	65	52
P2.2	INT2	I	External Interrupt 2	46	66	53
P2.2	SCK	O	SPI Serial Clock	46	66	53
P2.3	SDO	O	SPI Serial Data In	47	67	54
P2.4	INT1	I	External Interrupt 1	48	68	
P2.4	$\overline{WRSTB5}$	I	Handshake Write Strobe P5	48	68	
P2.5	WRRDY5	O	Handshake Write Ready P5	49	69	
P2.6	INT3	I	External Interrupt 3	50	70	
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50	70	
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50	70	
P2.7	RDRDY5	O	Handshake Read Ready P5	51	71	
P3.0	T0INA	I	MF Timer 0 Input A	15	29	27
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15	29	27
P3.1	T0OUTA	O	MF Timer 0 Output A	14	28	26
P3.2	T0INB	I	MF Timer 0 Input B	13	27	25
P3.3	T0OUTB	O	MF Timer 0 Output B	12	26	24
P3.4	T1INA	I	MF Timer 1 Input A	11	25	23

PIN DESCRIPTION (Continued)

Table 4. ST9040 I/O Port Alternate Function Summary(Continued)

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
Port. bit				PLCC	PQFP	PSDIP
P3.5	T1OUTA	O	MF Timer 1 Output A	10	24	22
P3.6	T1INB	I	MF Timer 1 Input B	9	23	20
P3.7	T1OUTB	O	MF Timer 1 Output B	8	22	19
P4.0	AIN0	I	A/D Analog Input 0	52	72	55
P4.1	AIN1	I	A/D Analog Input 1	53	73	56
P4.2	AIN2	I	A/D Analog Input 2	54	74	1
P4.3	AIN3	I	A/D Analog Input 3	55	75	2
P4.4	AIN4	I	A/D Analog Input 4	61	4	8
P4.5	AIN5	I	A/D Analog Input 5	56	76	3
P4.6	AIN6	I	A/D Analog Input 6	57	77	4
P4.7	AIN7	I	A/D Analog Input 7	58	78	5
P5.0		I/O	I/O Handshake Port 5	3	15	
P5.1		I/O	I/O Handshake Port 5	2	14	
P5.2		I/O	I/O Handshake Port 5	1	13	14
P5.3		I/O	I/O Handshake Port 5	68	11	13
P5.4		I/O	I/O Handshake Port 5	65	8	12
P5.5		I/O	I/O Handshake Port 5	64	7	11
P5.6		I/O	I/O Handshake Port 5	63	6	10
P5.7		I/O	I/O Handshake Port 5	62	5	9
P7.0	SIN	I	SCI Serial Input	43	61	50
P7.1	SOUT	O	SCI Serial Output	42	60	49
P7.1	ROMless	I	ROMless Select (Mask option)	42	60	49
P7.2	INT4	I	External Interrupt 4	41	59	48
P7.2	TXCLK	I	SCI Transmit Clock Input	41	59	48
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41	59	48
P7.3	INT5	I	External Interrupt 5	40	58	47
P7.3	RXCLK	I	SCI Receive Clock Input	40	58	47
P7.3	ADTRG	I	A/D Conversion Trigger	40	58	47
P7.4	INT6	I	External Interrupt 6	39	57	
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39	57	
P7.5	$\overline{WAIT}$	I	External Wait Input	38	56	
P7.6	WDOUT	O	T/WD Output	37	55	46
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37	55	46
P7.7	WDIN	I	T/WD Input	36	54	45
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36	54	45

ADDRESS SPACES

Table 1-5. Group F Peripheral Organization

Applicable for ST9040

DEC	HEX	00	02	03	08	09	10	24	63	
		00	02	03	08	09	0A	18	3F	
R255	RFF	RESERVED	RESERVED					RESERVED		RFF
R254	RFE	MSPI	PORT 3	PORT 7						RFE
R253	RFD					RESERVED				RFD
R252	RFC	WCR								RFC
R251	RFB		RESERVED							RFB
R250	RFA	T/WD		RESERVED						RFA
R249	RF9		PORT 2		MFT 1		MFT 0		A/D	RF9
R248	RF8					MFT				RF8
R247	RF7		RESERVED							RF7
R246	RF6			PORT 5		MFT 1		SCI		RF6
R245	RF5	EXT INT	PORT1							RF5
R244	RF4									RF4
R243	RF3		RESERVED	RESERVED						RF3
R242	RF2					MFT0				RF2
R241	RF1	EEPROMCR	PORT 0	PORT 4						RF1
R240	RF0	RESERVED								RF0

1.3 MEMORY

1.3.1 INTRODUCTION

The memory of the ST9 is divided into two spaces:

- Data memory with up to 64K (65536) bytes
- Program memory with up to 64K (65536) bytes

Thus, there is a total of 128K bytes of addressable memory space.

The 16K bytes of on-chip ROM memory of the ST9040 are selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space.

The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of on-chip RAM memory at addresses 200h through 2FFh.

1.3.2 EEPROM

1.3.2.1 Introduction

The EEPROM memory provides user-programmable non-volatile memory on-chip, allowing fast and reliable storage of user data. As there is also no off-chip access required, as for an external serial EEPROM, high security levels can be achieved.

The EEPROM memory is read as normal RAM memory at Data Space addresses 0 to 1FFh, however one WAIT cycle is automatically added for a Read cycle, while a byte write cycle to the EEPROM will cause the start of an ERASE/WRITE cycle at the addressed location. Word (16 bit) writes are not allowed.

The programming cycle is self-timed, with a typical programming time of 6ms. The voltage necessary for programming the EEPROM is internally generated with a +18V charge pump circuit.

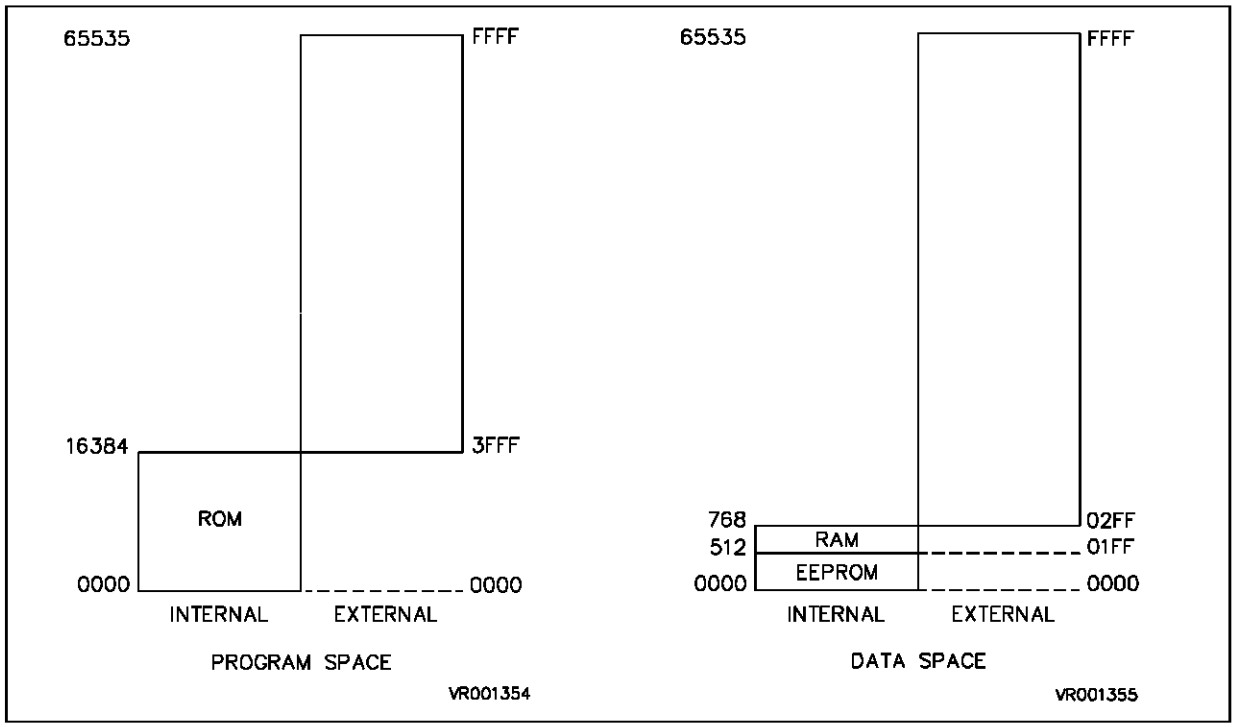
Up to 16 bytes of data may be programmed into the EEPROM during the same write cycle by using the PARALLEL WRITE function.

A standby mode is also available which disables all power consumption sources within the EEPROM for low power requirements. When STBY is high, any attempt to access the EEPROM memory will produce unpredictable results. After the re-enabling of the EEPROM, a delay of 6 INTCLK cycles must be allowed before the selection of the EEPROM.

The EEPROM of the ST9040 has been implemented in a high reliability technology developed by SGS-THOMSON, this, together with the double bit structure, allow 300k Erase/Write cycles and 10 year data retention to be achieved on a microcontroller.

Control of the EEPROM is performed through one register mapped at register address R241 in Page 0.

Figure 1-4. Memory Map



EEPROM (Continued)

1.3.2.2 EEPROM Programming Procedure
The programming of a byte of EEPROM memory is equivalent to writing a byte into a RAM location after verifying that EEBUSY bit is low. Instructions operating on word data (16 bits) will not access the EEPROM.

The EEPROM ENABLE bit EEWEN must first be set before writing to the EEPROM. When this bit is low, attempts to write data to the EEPROM have no affect, this prevents any spurious memory accesses from affecting the data in the EEPROM.

Termination of the write operation can be detected by polling on the EEBUSY status bit, or by interrupt, taking the interrupt vector from the External Interrupt 4 channel. The selection of the interrupt is made by EEPROM Interrupt enable bit EEIEN. It should be noted that the Mask bit of External Interrupt 4 should be set, and the Interrupt Pending bit reset, before the setting of EEIEN to prevent unwanted interrupts. A delay (eg a nop instruction) should also be included between the operations on the mask and pending bits of External Interrupt 4.

If polling on EEBUSY is used, a delay of 6 INTCLK clock cycles is necessary after the end of programming, this can be a nop instruction or, normally, therequired time to test the EEBUSY bit and to branch to the next instruction will be sufficient. While EEBUSY is active, any attempt to access the EEPROM matrix will be aborted and the data read will be invalid. EEBUSY is a read only bit and cannot be reset by the user if active.

An erased bit of the EEPROM memory will read as a logic “0”, while a programmed cell will be read as a logic “1”. For applications requiring the highest level of reliability, the Verify Mode, set by EEPROM control register bit VRFY, allows the reading of the EEPROM memory cells with a reduced gate voltage (typically 20%). If the EEPROM memory cell has been correctly programmed, a logic “1” will be read with the reduced voltage, otherwise a logic “0” will be read.

1.3.2.3 Parallel Programming Procedure
Parallel programming is a feature of the EEPROM macrocell. One up to sixteen bytes of a same row can be programmed at once.

The constraint is that each of the bytes occur in the same ROW of the EEPROM memory (A4 constant, A3-A0 variable). To operate this mode, the Parallel Mode enable bit, PLLEN, must be set. The data written is then latched into buffers (at the addresses specified, which may be non-sequential) and then transferred to the EEPROM memory by the setting of the PLLST bit of the control register. Both PLLST and PLLEN are internally reset at the end of the programming cycle. Any attempt to read the EEPROM memory when PLLEN is set will give invalid data. In the event that the data in the buffer latches is not required to be written into the memory by the setting of PLLST, the correct way to terminate the operation is to reset PLLEN and to perform a dummy read of the EEPROM memory. This termination will clear all data present in the latches.

1.3.2.4 EEPROM Programming Voltage
No external Vpp voltage is required, an internal 18Volt charge-pump gives the required energy by a dedicated oscillator pumping at a typical frequency of 5MHz, regardless of the external clock.

1.3.2.5 EEPROM Programming Time
No timing routine is required to control the programming time as dedicated circuitry takes care of the EEPROM programming time (The typical programming time is 6ms).

1.3.2.6 EEPROM Interrupt Management
At the end of each write procedure the EEPROM sends an interrupt request (if EEIEN bit is set). The EEPROM shares its interrupt channel with the external interrupt source INT4, from which the priority level is derived.

Care must be taken when EEIEN is reset. The associated external interrupt channel must be disabled (by reseting bit 4 of EIMR, R244) along with reseting the interrupt pending bit (bit 4 of EIPR, R243) to prevent unwanted interrupts. A delay instruction (at least 1 nop instruction) must be inserted between these two operations

WARNING. *The content of the EEPROM of the ST9040 family after the out-going test at SGS-THOMSON’s manufacturing location is not guaranteed.*

EEPROM (Continued)

1.3.2.7 EEPROM Control Register
EECR R241 (F1h) Page 0 Read/Write (except EEBUSY: read only)
EEPROM Control Register

Reset value : 0000 0000b (00h)

7							0
0	VERIFY	EESTBY	EEIEN	PLLST	PLLEN	EEBUSY	EEWEN

bit 7 = **B7:** This bit is forced to "0" after reset and **MUST** not be modified by the user.

bit 6 = **VERIFY:** *Set Verify mode*. Verify (active high) is used to activate the verify mode.

The verify mode provides a guarentee of good retention of the programmed bit. When active, the reading voltage on the cell gate is decreased from 1.2V to 0.0V, decreasing the current from the programmed cell by 20%. If the cell is well programmed (to "1"), a "1" will still be read, otherwise a "0" will be read.

Note . The verify mode must not be used during an erasing or a programming cycle).

bit 5 = **EESTBY:** *EEPROM Stand-By*. EESTBY = "1" switches off all power consumption sources inside the EEPROM. Any attempt to access the EEPROM when EESTBY = "1" will produce unpredictable results.

Note. After EESTBY is reset, the user must wait 6 CPUCLK cycles (e.g. 1 nop instruction) before selecting the EEPROM.

bit 4 = **EEIEN:** *EEPROM Interrupt Enable*. INTEN = "1" disables the external interrupt source INT4, and enables the EEPROM to send its interrupt request to the central interrupt unit at the end of each write procedure.

bit 3 = **PLLST:** *Parallel Write Start*. Setting PLLST to "1" starts the parallel writing procedure. It can be set only if PLLEN is already set. PLLST is internally reset at the end of the programming sequence.

bit 2 = **PLLEN:** *Parallel write Enable*. Setting PLLEN to "1" enables the parallel writing mode which allows the user to write up to 16 bytes at the same time. PLLEN is internally reset at the end of the programming sequence.

bit 1 = **EEBUSY:** *BUSY*. When this read only bit is high, an EEPROM write operation is in progress and any attempt to access the EEPROM is aborted.

bit 0 = **EEWEN:** *EEPROM Write Enable*. Setting this bit allows programming of the EEPROM, when low a writing attempt has no effect.

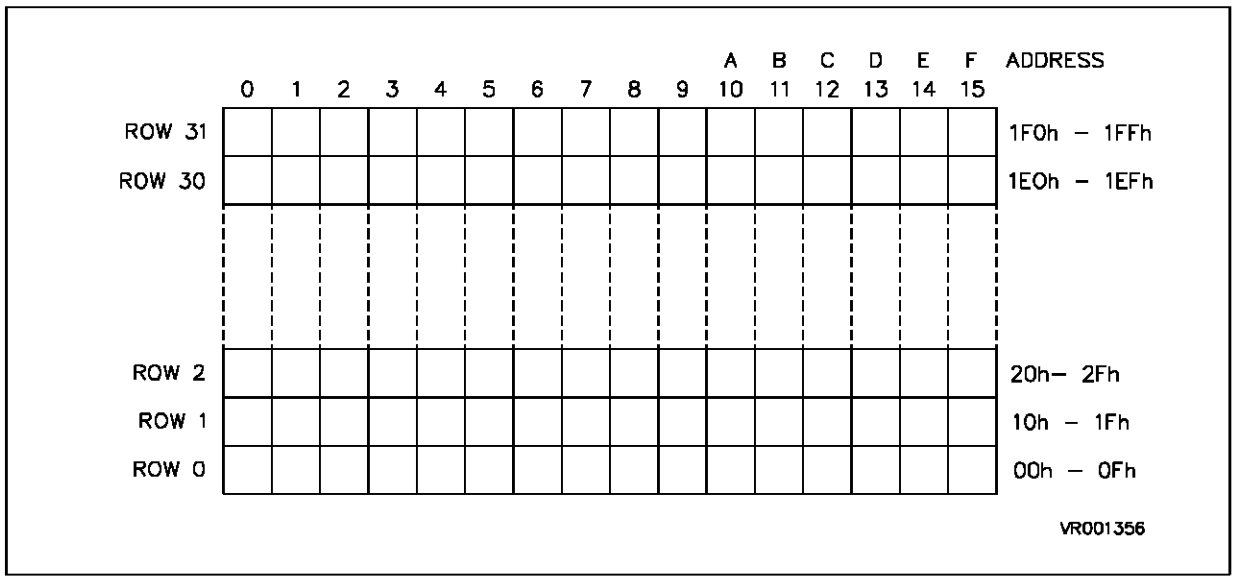
1.3.3 REGISTER MAP

Please refer to the Register Map of the ST9030 for all general registers with the exception of the register shown in the following table.

Table 1-6. Register Map Addendum

EECR	R241	(F1h)	Page 0	Read/Write	Control Registers

Figure 1-5. EEPROM Parallel Programming Rows



2 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} = AV_{SS} < AV_{DD} \leq V_{DD}$	V
V_I	Input Voltage	– 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	– 0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature	– 55 to + 150	°C
I_{INJ}	Pin Injection Current Digital Input	-5 to +5	mA
I_{INJ}	Pin Injection Current Analog Input	-5 to +5	mA
	Maximum Accumulated Pin injection Current in the device	-50 to +50	mA

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. All voltages are referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Clock Frequency (INTCLK)		12	MHz

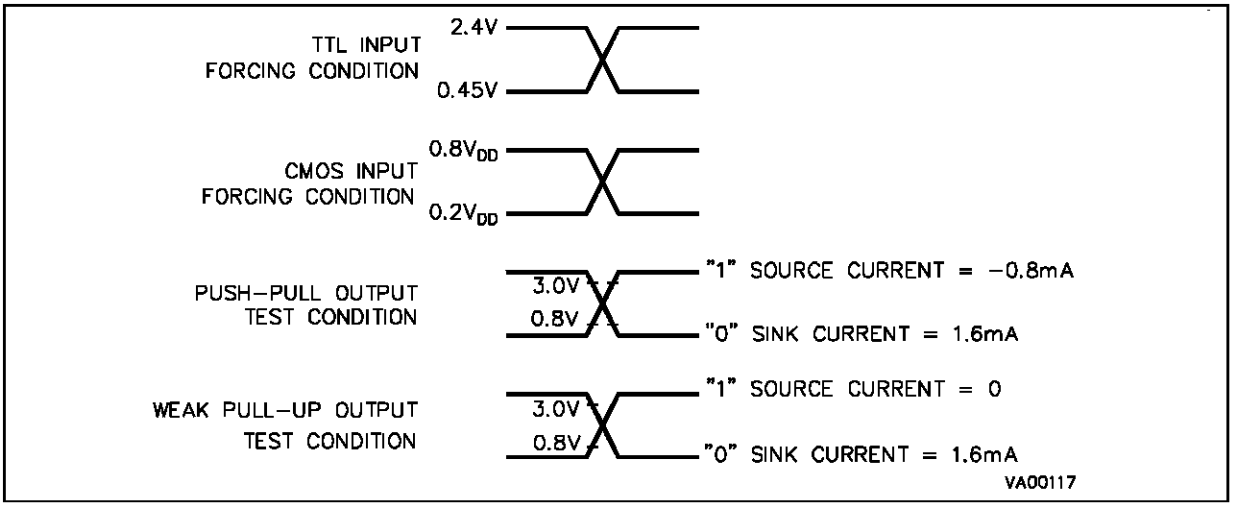
DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	$\overline{\text{RESET}}$ Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	$\overline{\text{RESET}}$ Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	$\overline{\text{RESET}}$ Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = 1.6mA			0.4	V
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 50	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V, under Reset	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, 0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{LKRS}	$\overline{\text{Reset}}$ Pin Input Leakage	0V < V_{IN} < V_{DD}	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, 0V < V_{IN} < V_{DD}	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	0V < V_{IN} < 0.8V	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	0V < V_{IN} < V_{DD}	– 10		+ 10	µA

Note: All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working.

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{DD}	Run Mode Current no CPUCLK prescale, Clock divide by 2	24MHz, Note 1			50	mA
I_{DP2}	Run Mode Current Prescale by 2 Clock divide by 2	24MHz, Note 1			30	mA
I_{WFI}	WFI Mode Current no CPUCLK prescale, Clock divide by 2	24MHz, Note 1			20	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA

Note 1: All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working.

CLOCK TIMING TABLE

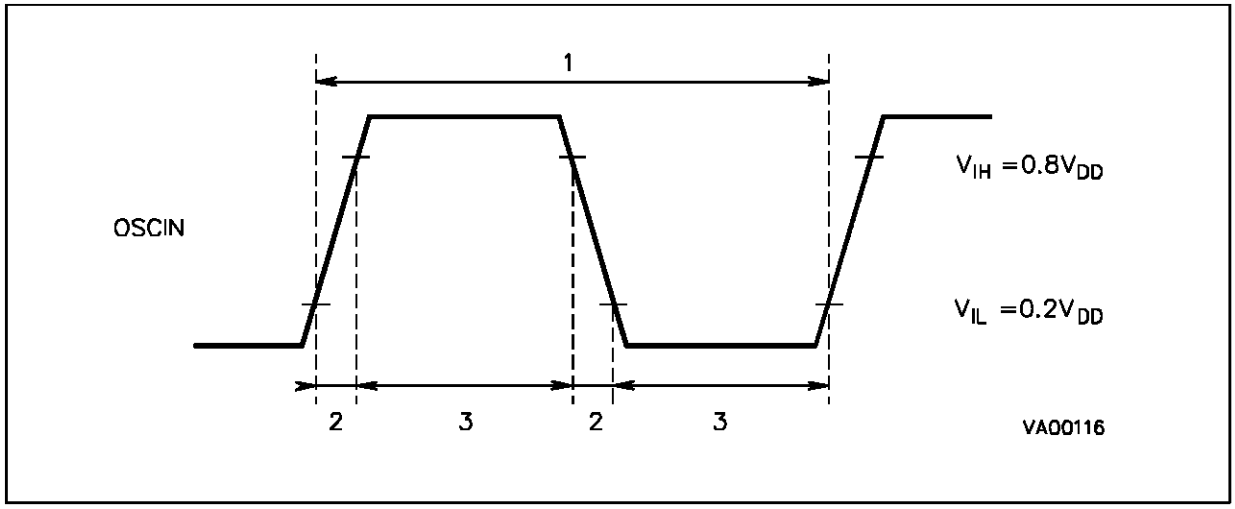
(V_{DD} = 5V ± 10%, T_A = – 40°C to + 85°C, INTCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	17	25	ns	1
			38		ns	2

Notes:

1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}\uparrow$	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}\uparrow$	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}\uparrow$ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}\downarrow$ t	12	12	12		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}\downarrow$ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) –46		75	ns
9	ThDR (DS)	Data to $\overline{DS}\uparrow$ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}\uparrow$ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}\uparrow$ to $\overline{AS}\downarrow$ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}\uparrow$	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}\uparrow$ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}\downarrow$ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after $\overline{DS}\uparrow$ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}\uparrow$ to $\overline{DS}\downarrow$ Delay	TpC –18	TwCL –14	24		ns

EXTERNAL WAIT TIMING TABLE

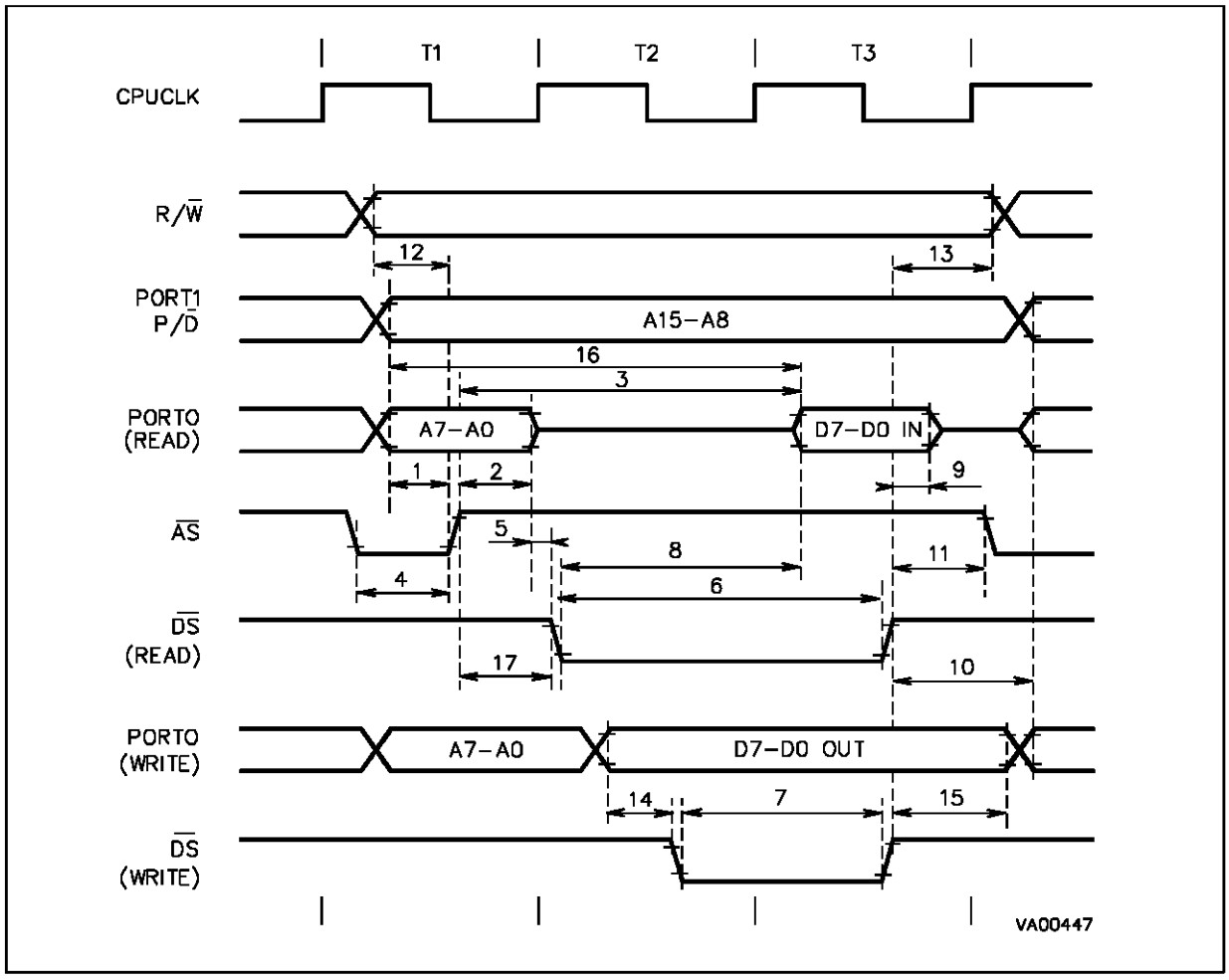
(V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF,
INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAs (WAIT)	$\overline{AS}\uparrow$ to $\overline{WAIT}\downarrow$ Delay	2(P+1)TpC –29	2(P+1)TpC –29		40	ns
2	TdAs (WAIT)	$\overline{AS}\uparrow$ to $\overline{WAIT}\downarrow$ Min. Delay	2(P+W+1)TpC –4	2(P+W+1)TpC –4	80		ns
3	TdAs (WAIT)	$\overline{AS}\uparrow$ to $\overline{WAIT}\downarrow$ Max. Delay	2(P+W+1)TpC –29	2(P+W+1)TpC –29		83W+ 40	ns

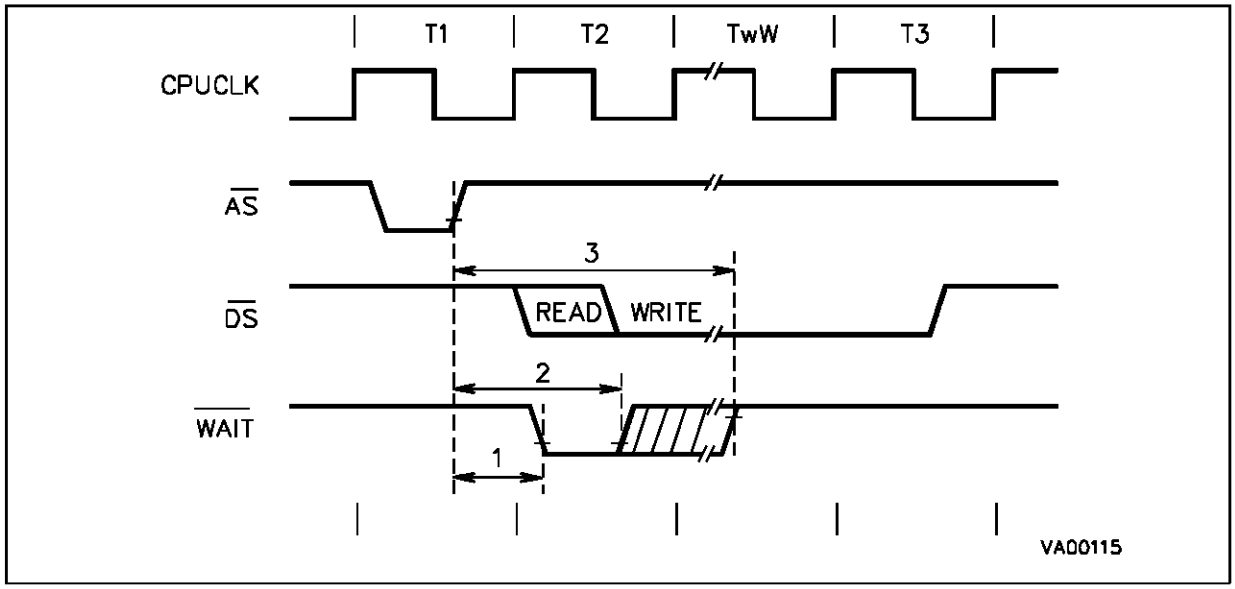
Note: (for both tables) The value in the left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value in the right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING



HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		TpC (P+W+1) – 18		65		ns
2	TwSTB	$\overline{\text{RDSTB}}$, $\overline{\text{WRSTB}}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{\text{RDSTB}}$, or $\overline{\text{WRSTB}}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+ (W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{\text{WRSTB}}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to $\overline{\text{WRSTB}}$ ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{\text{RDSTBD}}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{\text{RDSTB}}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

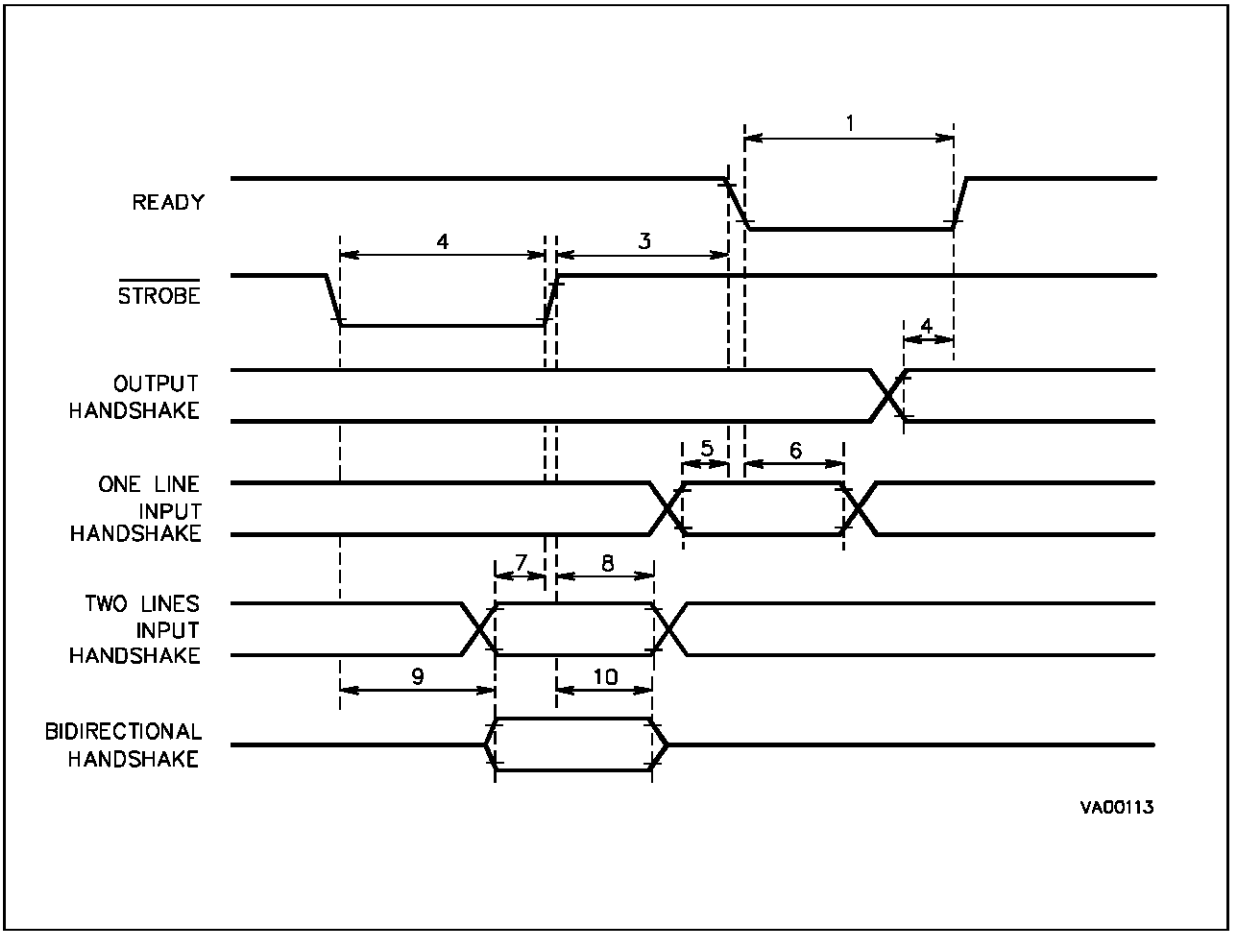
Note: The value in the left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value in the right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:

P = Clock Prescaling Value (R235.4,3,2)

W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

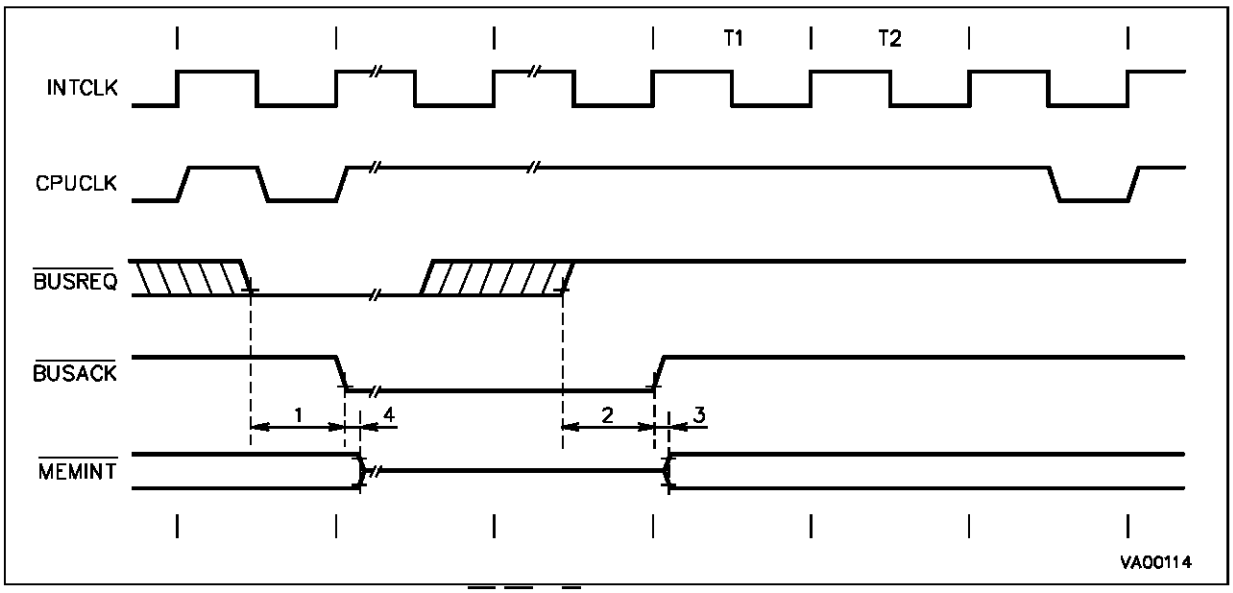


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}\downarrow$ to $\overline{BUSACK}\downarrow$	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}\uparrow$ to $\overline{BUSACK}\uparrow$	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}\downarrow$ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}\uparrow$ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



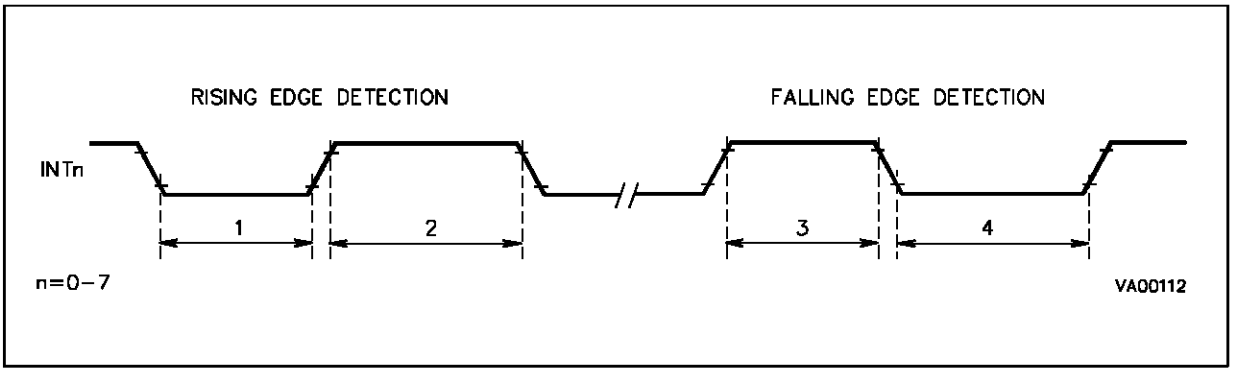
Note : MEMINT = Group of memory interface signals: $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17

EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL INTERRUPT TIMING

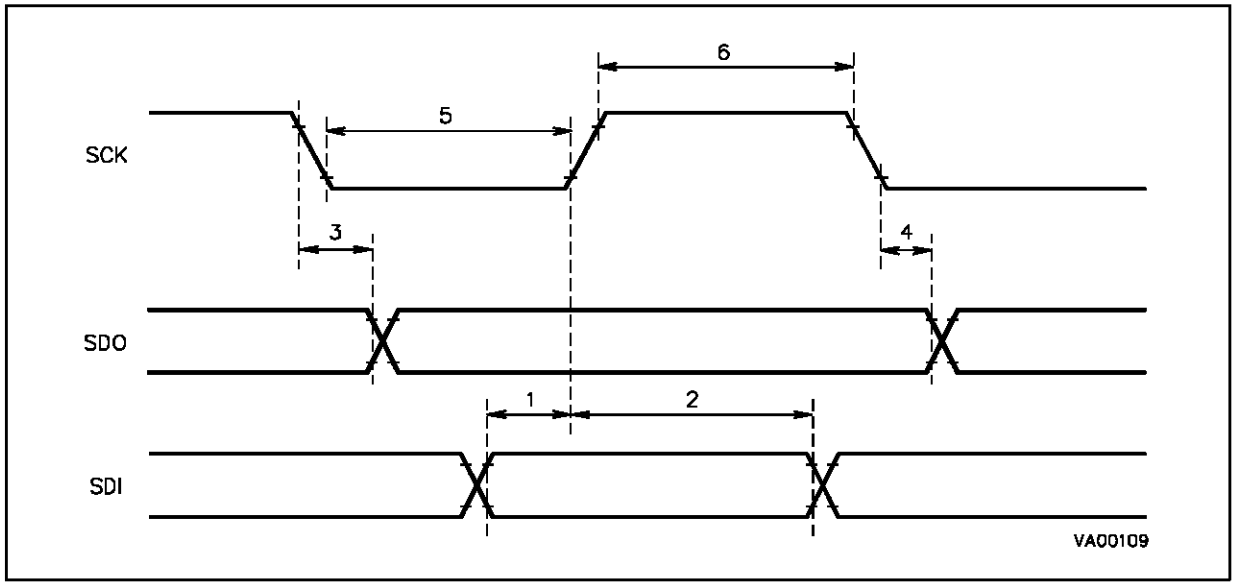


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

Note: TpC is the OSCIN Clock period.

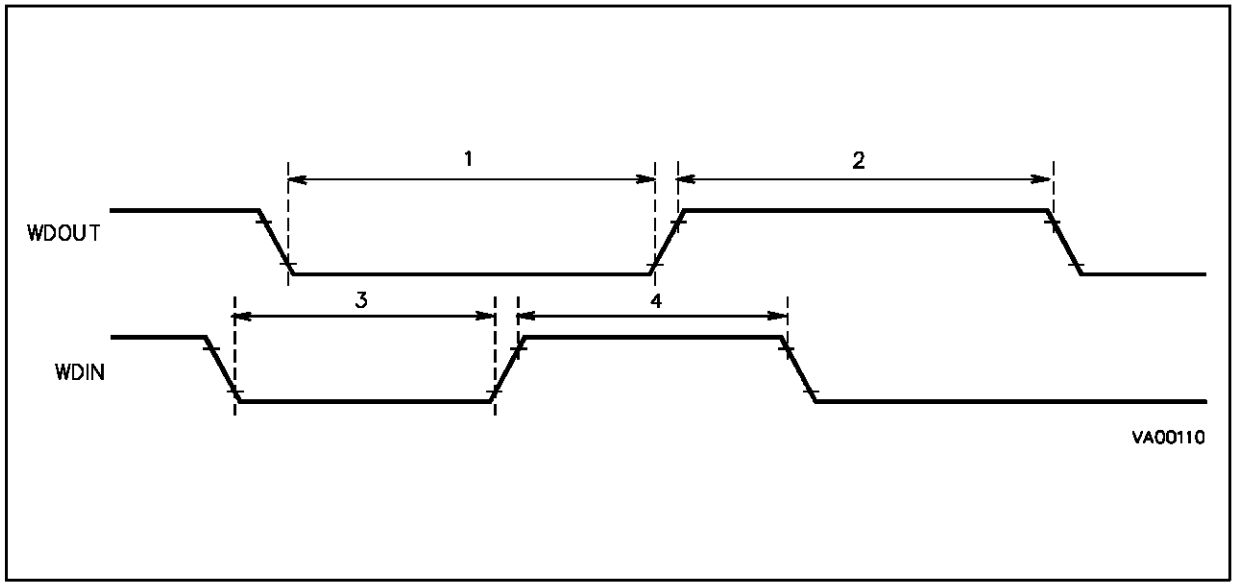
SPI TIMING



WATCHDOG TIMING TABLE(V_{DD} = 5V ± 10%, T_A = – 40 °C to +85°C, Cload = 50pF, CPUCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Values		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN High Pulse Width	350		ns
4	TwWDIH	WDIN Low Pulse Width	350		ns

WATCHDOG TIMING



A/D CONVERTER

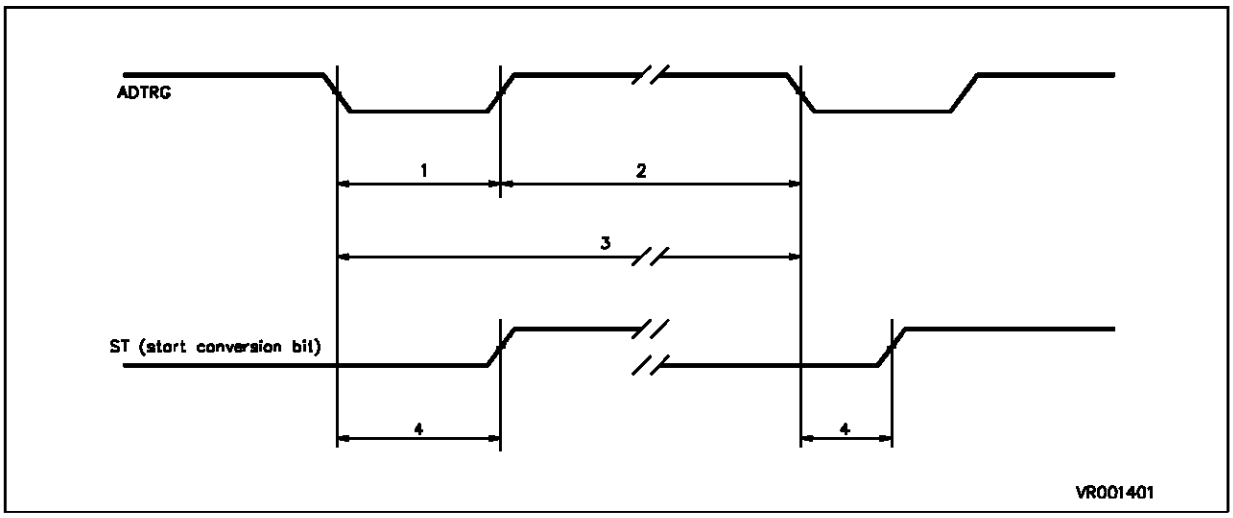
EXTERNAL TRIGGER TIMING (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF)

N°	Symbol	Parameter	Oscin divided by 2 (1)		Oscin not divided (1)		Value(2)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	T_{LOW}	External Trigger pulse width	$2xT_{PC}$		T_{PC}		83		ns
2	T_{HIGH}	External Trigger pulse	$2xT_{PC}$		T_{PC}		83		ns
3	T_{EXT}	External trigger active edges distance	$138xT_{PC}$		$69xT_{PC}$		5.75		µs
4	T_{STR}	Internal delay between EXTRG falling edge and first conversion start	T_{PC}	$3xT_{PC}$	0.5xTPC	$1.5xT_{PC}$	41.5	125	ns

Notes:

1. Variable clock (T_{PC}=OSCIN clock period)
2. INTCLK=12MHz

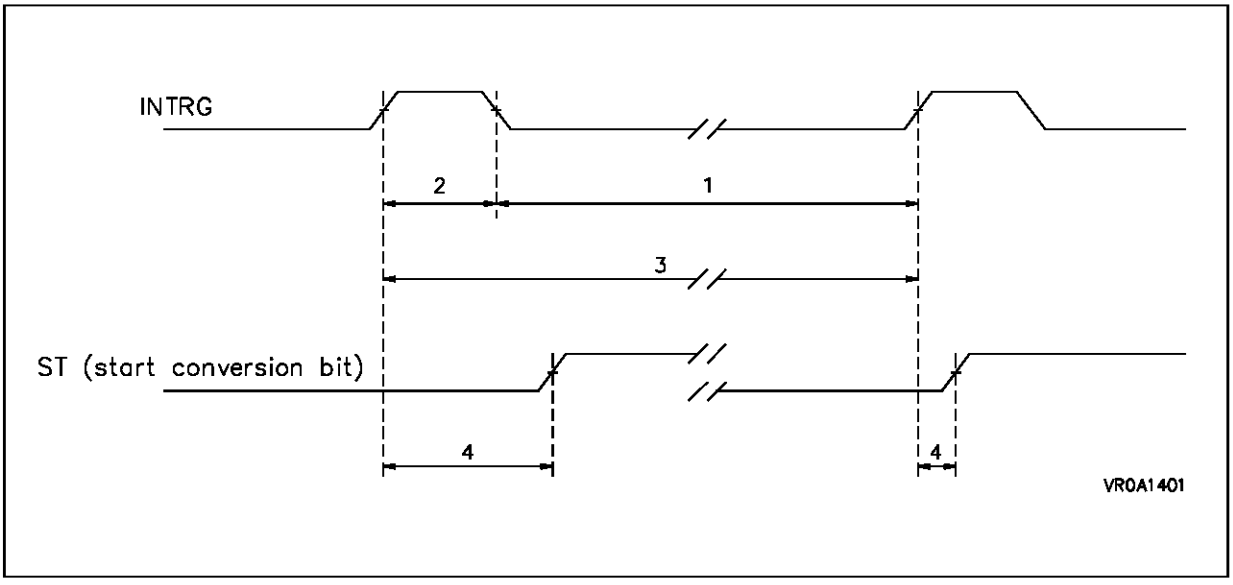
A/D External Trigger Timing



A/D INTERNAL TRIGGER TIMING TABLE

N°	Symbol	Parameter	OSCIN Divided by 2 (2)		OSCIN Not Divided by 2 (2)		Value (3)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	Tw_{HIGH}	Internal trigger pulse width	Tpc		.5 x Tpc		41.5	-	ns
2	Tw_{LOW}	Internal trigger pulse distance	6 x Tpc		3 x Tpc		250	-	ns
3	Tw_{EXT}	Internal trigger active edges distance (1)	276n x Tpc		138n x Tpc		n x 11.5	-	µs
4	Tw_{STR}	Internal delay between INTRG rising edge and first conversion start	Tpc	3 x Tpc	.5 x Tpc	1.5 x Tpc	41.5	125	ns

A/D INTERNAL TRIGGER TIMING



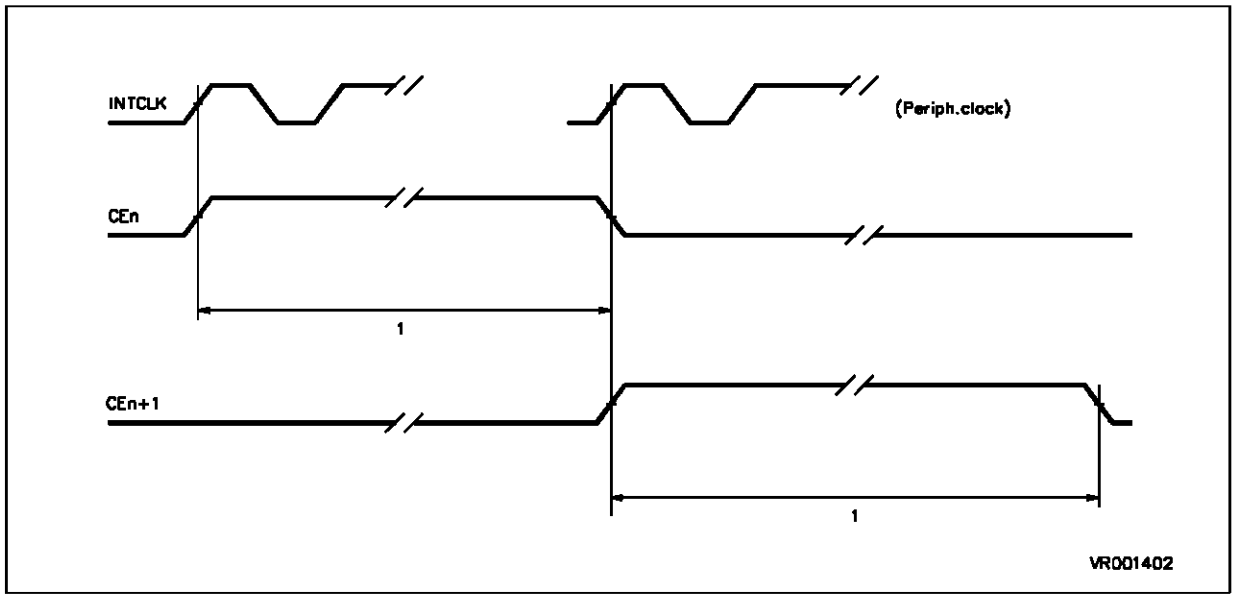
A/D CHANNEL ENABLE TIMING TABLE

N°	Symbol	Parameter	OSCIN Divided by 2 (2)		OSCIN Not Divided by 2 (2)		Value (3)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	Tw_{EXT}	CEn Pulse width (1)	276n x Tpc		138n x Tpc		n x 11.5	-	µs

Notes:

1. n = number of autoscanned channels (1 < n < 8)
2. Variable clock (Tpc = OSCIN clock period)
3. CPUCLK = 12MHz

A/D CHANNEL ENABLE TIMING



A/D ANALOG SPECIFICATIONS

Parameter	Typical (1)	Minimum	Maximum	Units (2)	Notes
Analog Input Range A_{VCC}		3	A_{VCC} V_{CC}	V	
Conversion time		11.5		µs	(3, 4)
Sample time		3		µs	(3)
Power-up time		60		µs	
Resolution	8	8		βιτσ	
Monotonicity	GUARANTEED				
No missing codes	GUARANTEED				
Zero input reading		00		Hex	
Full scale reading			FF	Hex	
Offset error	.5		1	LSBs	(2,6)
Gain error	.5		1	LSBs	(6)
Diff. Non Linearity	±.3	±.2	±.5	LSBs	(6)
Int. Non Linearity			1	LSBs	(6)
Absolute Accuracy			1	LSBs	(6)
S/N		45	49	dB	
A_{VCC}/A_{VSS} Resistance	13.5	16	11	KΩ	
Input Resistance	12	8	15	KΩ	(5)
Hold Capacitance			30	pF	
Input Leakage			±3	µA	

Notes:

1. The values are expected at 25 degree Centigrade with $A_{VCC} = 5V$
2. "LSBs", as used here, has a value of $A_{VCC}/256$
3. @ 12MHz internal clock
4. Including sample time
5. It must be intended as the internal series resistance before the sampling capacitor
6. This is a typical expected value, but not a tested production parameter.
   If V(i) is the value of the i-th transition level ($0 < i < 254$), the performance of the A/D converter has been valued as follows:

   OFFSET ERROR = deviation between the actual V(0) and the ideal V(0) (=1/2 LSB)

   GAIN ERROR = deviation between the actual V(254) and the ideal V(254) (=AVCC-3/2 LSB)

   DNL ERROR = max {[V(i) - V(i-1)]/LSB - 1}

   INL ERROR = max {[V(i) - V(0)]/LSB - i}

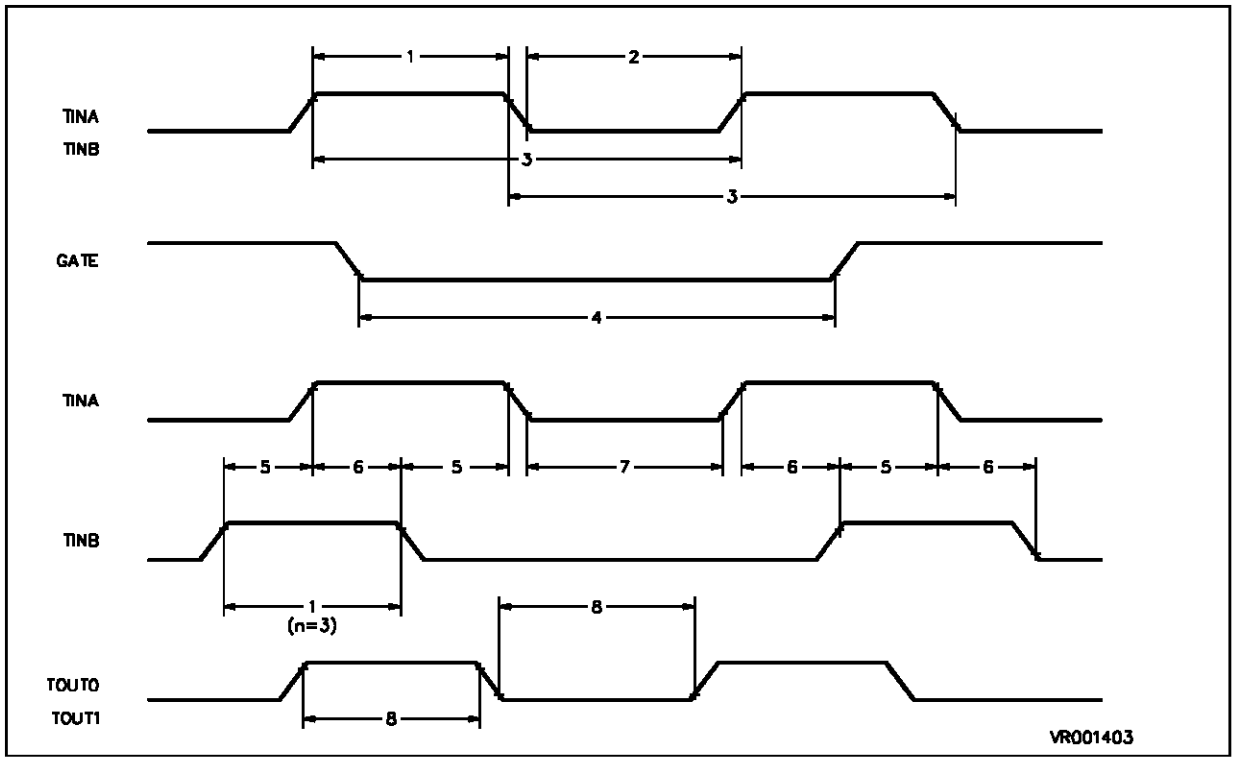
MULTIFUNCTION TIMER UNIT EXTERNAL TIMING TABLE

N°	Symbol	Parameter	OSCIN Divided by 2 (3)	OSCIN Not Divided by 2 (3)	Value (4)		Unit	Note
					Min.	Max.		
1	Tw_{CTW}	External clock/trigger pulse width	2n x Tpc	n x Tpc	n x 83	-	ns	1
2	Tw_{CTD}	External clock/trigger pulse distance	2n x Tpc	n x Tpc	n x 83	-	ns	1
3	Tw_{AED}	Distance between two active edges	6 x Tpc	3 x Tpc	249	-	ns	
4	Tw_{GW}	Gate pulse width	12 x Tpc	6 x Tpc	498	-	ns	
5	Tw_{LBA}	Distance between TINB pulse edge and the following TINA pulse edge	2 x Tpc	Tpc	83	-	ns	2
6	Tw_{LAB}	Distance between TINA pulse edge and the following TINB pulse edge	0		0	-	ns	2
7	Tw_{AD}	Distance between two TxINA pulses	0		0	-	ns	2
8	Tw_{OWD}	Minimum output pulse width/distance	6 x Tpc	3 x Tpc	249	-	ns	

Notes:

1. n = 1 if the input is rising OR falling edge sensitive
   n = 3 if the input is rising AND falling edge sensitive
2. In Autodiscrimination mode
3. Variable clock (Tpc = OSCIN period)
4. INTCLK = 12 MHz

MULTIFUNCTION TIMER UNIT EXTERNAL TIMING



SCI TIMING TABLE
(V_{DD} = 5V ± 10%, T_A = - 40°C to +85°C, Cload = 50pF, INTCLK = 12MHz,
Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Condition	Value		Unit
				Min.	Max.	
	F_{RxCKIN}	Frequency of RxCKIN	1 x mode		$F_{CK}/8$	Hz
			16 x mode		$F_{CK}/4$	Hz
	TW_{RxCKIN}	RxCKIN shortest pulse	1 x mode	4 T_{CK}		s
			16 x mode	2 T_{CK}		s
	F_{TxCKIN}	Frequency of TxCKIN	1 x mode		$F_{CK}/8$	Hz
			16 x mode		$F_{CK}/4$	Hz
	TW_{TxCKIN}	TxCKIN shortest pulse	1 x mode	4 T_{CK}		s
			16 x mode	2 T_{CK}		s
1	Ts_{DS}	DS (Data Stable) before rising edge of RxCKIN	1 x mode reception with RxCKIN	$T_{PC}/2$		ns
2	Td_{D1}	TxCKIN to Data out delay Time	1 x mode transmission with external clock C load <100pF		2.5 T_{PC}	ns
3	Td_{D2}	CLKOUT to Data out delay Time	1 x mode transmission with CLKOUT	350		ns

Note: $F_{CK} = 1/T_{CK}$

SCI TIMING

FIG 1: RECEPTION WITH EXTERNAL CLOCK 1X MODE

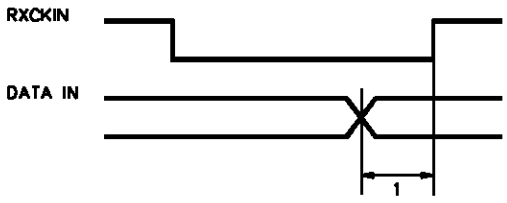


FIG 2: TRANSMISSION WITH EXTERNAL CLOCK 1X MODE

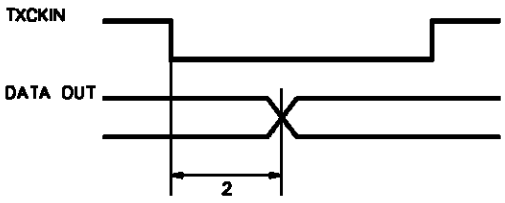
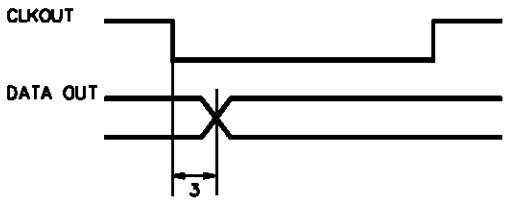


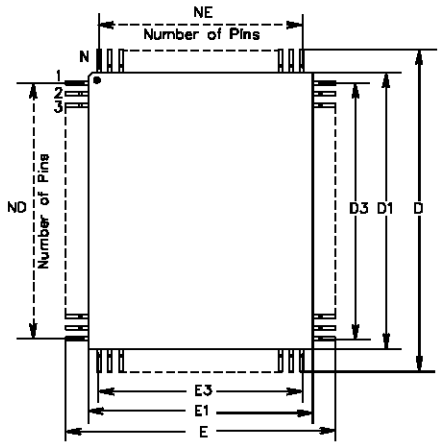
FIG 3: TRANSMISSION WITH CLKOUT 1X MODE



VR001437

PACKAGE MECHANICAL DATA

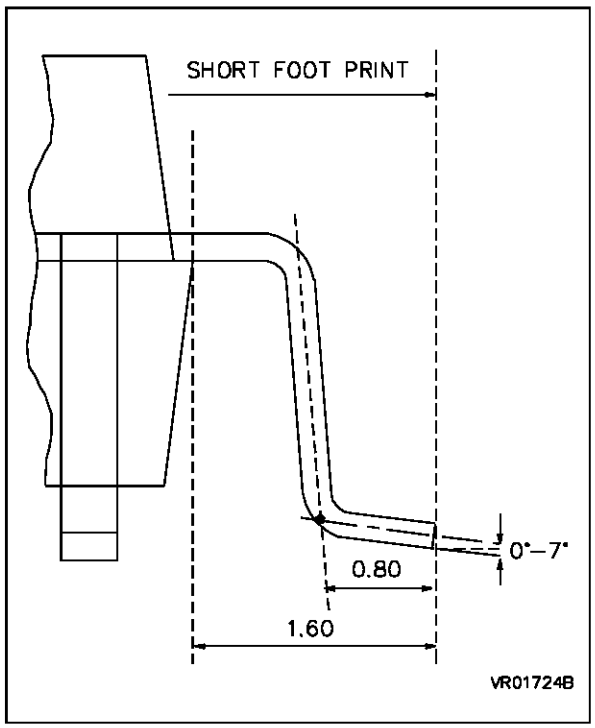
80-Pin Plastic Quad Flat Package



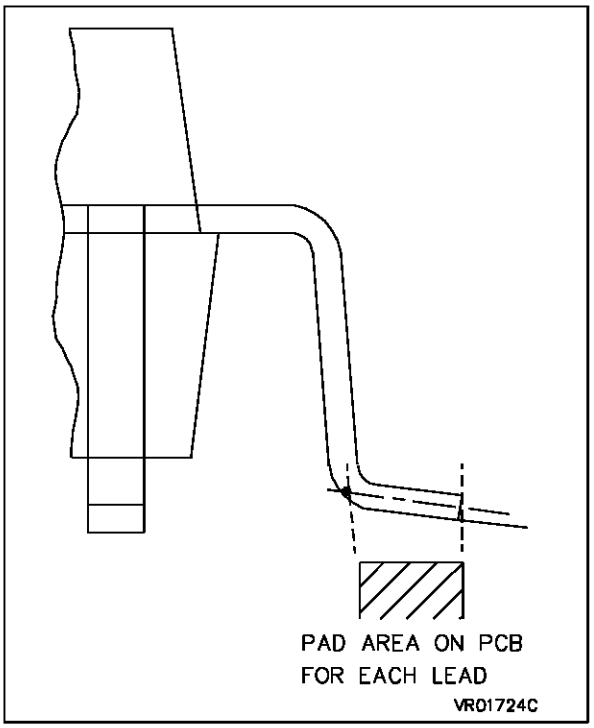
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.40			0.134
A2	2.55	2.80	3.05	0.100	0.110	0.120
D	22.95	23.20	24.45	0.903	0.913	0.923
D1	19.90	20.00	20.10	0.783	0.787	0.791
D3		18.40			0.724	
E	16.95	17.20	17.45	0.667	0.677	0.687
E1	13.90	14.00	14.10	0.547	0.551	0.555
E3		12.00			0.472	
e		0.80			0.032	

Number of Pins	
N	80
ND	24
NE	16

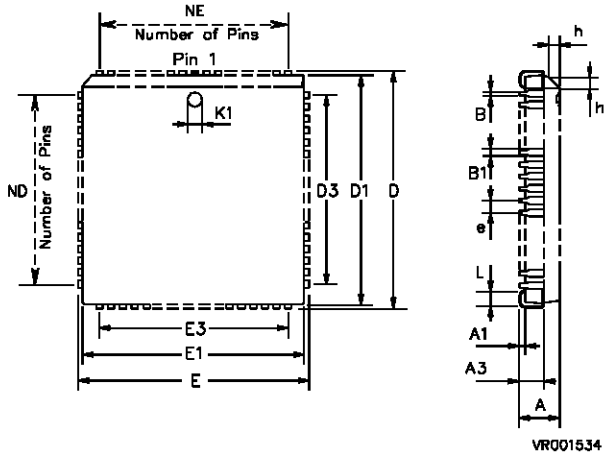
Short Footprint Measurement



Short Footprint recommended Padding

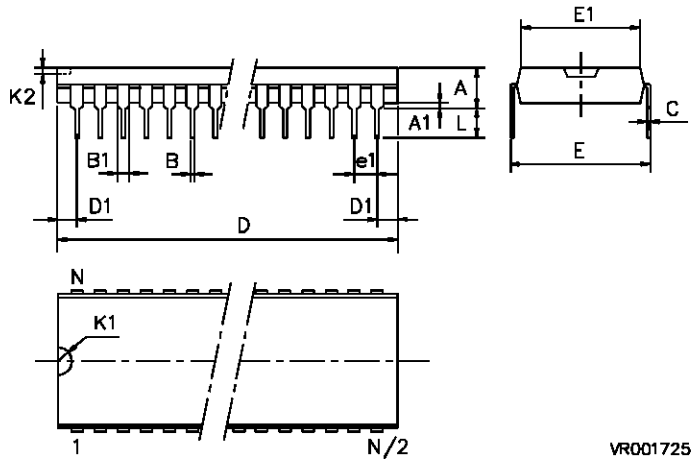


68-Pin Plastic Leadless Chip Carrier



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	4.20		5.08	0.165		0.200
A1	0.51			0.020		
A3	2.29		3.30	0.090		0.130
B	-	-	-	-	-	-
B1	-	-	-	-	-	-
D	25.02		25.27	0.985		0.995
D1	24.13		24.33	0.950		0.958
D3		20.32			0.800	
E	25.02		25.27	0.985		0.995
E1	24.13		24.33	0.950		0.958
E3		20.32			0.800	
K1	-	-	-	-	-	-
h						
e		1.27			0.050	
Number of Pins						
N	68					
ND	16					
NE	16					

56-Pin Plastic Shrink Dual-In-line Package, 600 Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			0.200
A1	0.51			0.020		
B	0.35		0.59	0.014		0.023
B1	0.75		1.42	0.030		0.056
C	0.20		0.36	0.008		0.014
D		52.12			2.052	
D1	–	–	–	–	–	–
E			18.54			0.730
E1		13.72				0.540
K1	–	–	–	–	–	–
K2	–	–	–	–	–	–
L	2.54		3.81	.100		0.150
e1		1.78			0.070	
Number of Pins						
N	56					

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST9040Q1/XX	24MHz	0°C to + 70°C	PQFP80
ST9040C1/XX			PLCC68
ST9040B1/XX			PSDIP56
ST9040C6/XX		-40°C to + 85°C	PLCC68
ST9040B6/XX			PSDIP56

Note: "XX" is the ROM code identifier that is allocated by SGS-THOMSON after receipt of all required options and the related ROM file.

ST9040 STANDARD OPTION LIST

Please copy this page (enlarge if possible) and complete ALL sections.
Send the form, with the ROM code image required, to your local SGS-THOMSON sales office.

Customer Company : [.....]
Company Address : [.....]
[.....]
Telephone : [.....]
FAX : [.....]
Contact : [.....] Telephone (Direct) : [.....]

Please confirm characteristics of device :

Device ST9040

Package [ ] PQFP80 [ ] PLCC68 [ ] PSDIP56

Temperature Range [ ] -40°C to +85°C [ ] 0°C to +70°C

Special Marking [ ] No
[ ] Yes 14 characters [| | | | | | | | | | | | |]
Authorized characters are letters, digits, '.', '-', '/' and spaces only.

Please consult your local SGS-THOMSON sales office for other marking details if required.

Notes :

ROMless Option (Consult text)
[ ] No
[ ] Yes Port Bit [ ] P7.1 [ ] P2.0

Code : [ ] EPROM (27128, 27256)
[ ] HEX format files on IBM-PC® compatible disk
filename : [.....]

Confirmation : [ ] Code checked with EPROM device in application

Yearly Quantity forecast : [.....] k units
- for a period of : [.....] years

Preferred Production start dates : [.....] (YY/MM/DD)

Customer Signature :

Date :

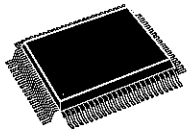
NOTES :

SGS-THOMSON MICROELECTRONICS

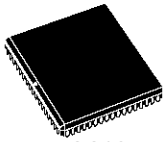
ST90E40
ST90T40

16K EPROM HCMOS MCU WITH EEPROM, RAM AND A/D CONVERTER

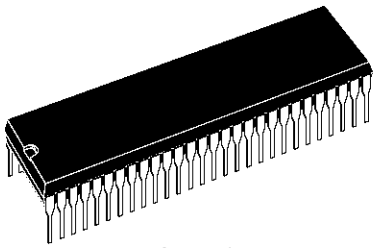
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- Internal Memory :
  EPROM 16Kbytes
  RAM 256 bytes
  EEPROM 512 bytes
  224 general purpose registers available as RAM, accumulators or index pointers (Register File)
- 80-pin Plastic Quad Flat Pack package for ST90T40Q
- 68-lead Plastic Leaded Chip Carrier package for ST90T40C
- 56-pin shrink DIP package for ST90T40B
- 80-pin Windowed Ceramic Quad Flat Pack package for ST90E40G
- 68-lead Windowed Ceramic Leaded Chip Carrier package for ST90E40L
- 56-pin Shrink Windowed Ceramic package for ST90E40D
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9036 and ST9040 16K ROM devices



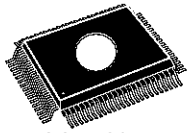
PQFP80



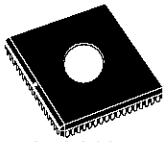
PLCC68



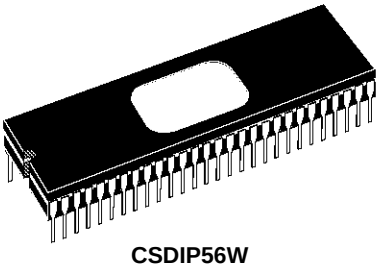
PSDIP56



CQFP80W



CLCC68W



CSDIP56W

(Ordering Information at the end of the Datasheet)

Figure 1. 80 Pin QFP Package

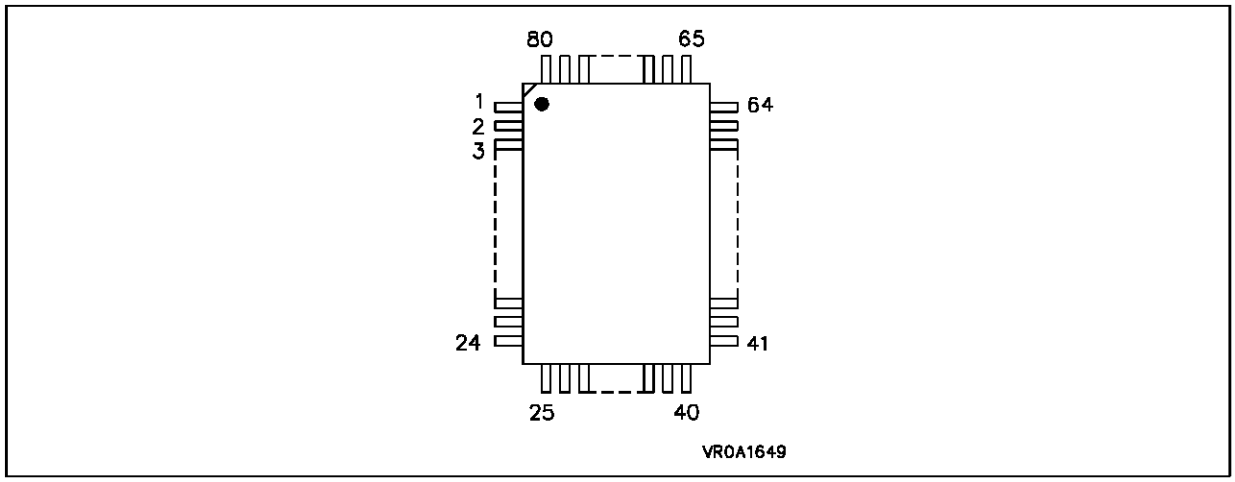


Table 1. ST90E40G-ST90T40Q Pin Description

Pin	Name
1	AV_{SS}
2	AV_{SS}
3	NC
4	P44/AIN4
5	P57
6	P56
7	P55
8	P54
9	INT7
10	INT0
11	P53
12	NC
13	P52
14	P51
15	P50
16	OSCOUT
17	V_{SS}
18	V_{SS}
19	NC
20	OSCIN
21	$\overline{RESET}/V_{PP}$
22	P37/T1OUTB
23	P36/T1INB
24	P35/T1OUTA

Pin	Name
25	P34/T1INA
26	P33/T0OUTB
27	P32/T0INB
28	P31/T0OUTA
29	P30/P/$\overline{D}$/T0INA
30	P17/A15
31	P16/A14
32	NC
33	P15/A13
34	P14/A12
35	P13/A11
36	P12/A10
37	P11/A9
38	P10/A8
39	P00/A0/D0
40	P01/A1/D1

Pin	Name
64	P20/NMI
63	NC
62	V_{SS}
61	P70/SIN
60	P71/SOUT
59	P72/INT4/TXCLK /CLKOUT
58	P73/INT5 /RXCLK/ADTRG
57	P74/P/$\overline{D}$/INT6
56	P75/$\overline{WAIT}$
55	P76/WDOUT /$\overline{BUSREQ}$
54	P77/WDIN /$\overline{BUSACK}$
53	R/$\overline{W}$
52	NC
51	$\overline{DS}$
50	$\overline{AS}$
49	NC
48	V_{DD}
47	V_{DD}
46	P07/A7/D7
45	P06/A6/D6
44	P05/A5/D5
43	P04/A4/D4
42	P03/A3/D3
41	P02/A2/D2

Pin	Name
80	AV_{DD}
79	NC
78	P47/AIN7
77	P46/AIN6
76	P45/AIN5
75	P43/AIN3
74	P42/AIN2
73	P41/AIN1
72	P40/AIN0
71	P27/RRDY5
70	P26/INT3 /$\overline{RDSTB5}$/P/$\overline{D}$
69	P25/WRRDY5
68	P24/INT1 /$\overline{WRSTB5}$
67	P23/SDO
66	P22/INT2/SCK
65	P21/SDI/P/$\overline{D}$

Figure 2. 68 Pin LCC Package

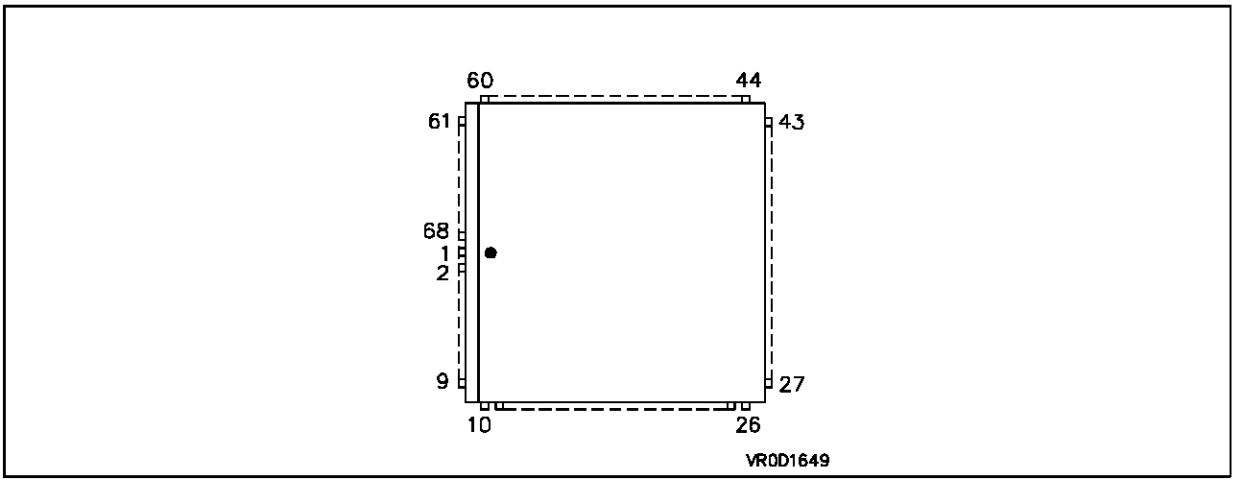


Table 2. ST90E40L-ST90T40C

Pin	Name
61	P44/AIN4
62	P57
63	P56
64	P55
65	P54
66	INT7
67	INT0
68	P53
● 1	P52
2	P51
3	P50
4	OSCOUT
5	V_{SS}
6	OSCIN
7	$\overline{RESET}/V_{PP}$
8	P37/T1OUTB
9	P36/T1INB

Pin	Name
10	P35/T1OUTA
11	P34/T1INA
12	P33/T0OUTB
13	P32/T0INB
14	P31/T0OUTA
15	P30/P/$\overline{D}$/T0INA
16	P17/A15
17	P16/A14
18	P15/A13
19	P14/A12
20	P13/A11
21	P12/A10
22	P11/A9
23	P10/A8
24	P00/A0/D0
25	P01/A1/D1
26	P02/A2/D2

Pin	Name
43	P70/SIN
42	P71/SOUT
41	P72/CLKOUT /TXCLK/INT4
40	P73/ADTRG /RXCLK/INT5
39	P74/P/$\overline{D}$/INT6
38	$\overline{P75/WAIT}$
37	P76/$\overline{WDOUT}$ /$\overline{BUSREQ}$
36	P77/$\overline{WDIN}$ /$\overline{BUSACK}$
35	R/$\overline{W}$
34	$\overline{DS}$
33	$\overline{AS}$
32	V_{DD}
31	P07/A7/D7
30	P06/A6/D6
29	P05/A5/D5
28	P04/A4/D4
27	P03/A3/D3

Pin	Name
60	AV_{SS}
59	AV_{DD}
58	P47/AIN7
57	P46/AIN6
56	P45/AIN5
55	P43/AIN3
54	P42/AIN2
53	P41/AIN1
52	P40/AIN0
51	P27/RRDY5
50	P26/$\overline{INT3}$ /$\overline{RDSTB5}$/P/$\overline{D}$
49	P25/WRRDY5
48	P24/$\overline{INT1}$ /$\overline{WRSTB5}$
47	P23/SDO
46	P22/INT2/SCK
45	P21/SDI/P/$\overline{D}$
44	P20/NMI

Figure 1b. 56 Pin Shrink DIP Pinout

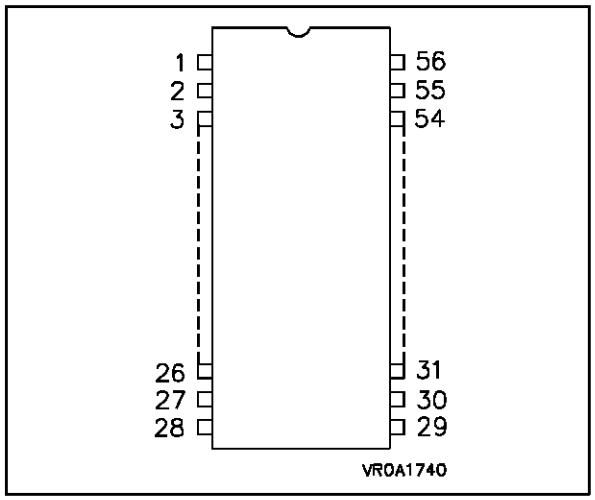


Table 3. ST90E40D-ST90T40B Pin Description

Pin	Pin name
1	P42/AIN2
2	P43/AIN3
3	P45/AIN5
4	P46/AIN6
5	P47/AIN7
6	AVDD
7	AVSS
8	P44/AIN4
9	P57
10	P56
11	P55
12	P54
13	P53
14	P52
15	OSCOUT
16	V_{SS}
17	OSCIN
18	$\overline{\text{RESET}}$
19	P37/T1OUTB
20	P36/T1INB
21	NC
22	P35/T1OUTA
23	P34/T1INA
24	P33/T0OUTB
25	P32/T0INB
26	P31/T0OUTA
27	P30/P/D/T0INA
28	P13/A11

Pin	Pin name
56	P41/AIN1
55	P40/AIN0
54	P23/SDO
53	P22/INT2/SCK
52	P21/SDI/P/$\overline{\text{D}}$
51	P20/NMI
50	P70/SIN
49	P71/SOUT
48	P72/CLKOUT TXCLK/INT4
47	P73/ADTRG RXCLK/INT5
46	P76WDOUT/$\overline{\text{BUSREQ}}$
45	P77/WDIN/BUSACK
44	R/$\overline{\text{W}}$
43	DS
42	$\overline{\text{AS}}$
41	V_{DD}
40	V_{SS}
39	P07/A7/D7
38	P06/A6/D6
37	P05/A5/D5
36	P04/A4/D4
35	P03/A3/D3
34	P02/A2/D2
33	P01/A1/D1
32	P00/A0/D0
31	P10/A8
30	P11/A9
29	P12/A10

1.1 GENERAL DESCRIPTION

The ST90E40 and ST90T40 (following mentioned as ST90E40) are EPROM members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

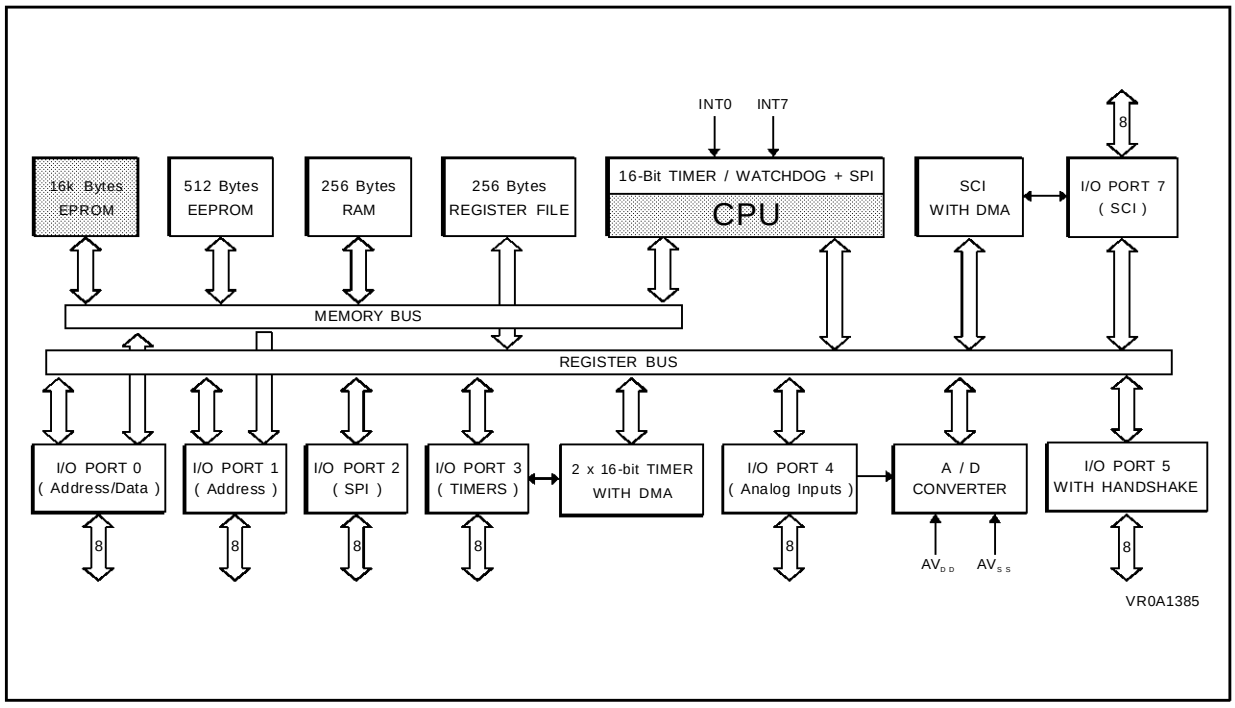
THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9040 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST90E40 may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip EPROM, a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

The nucleus of the ST90E40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E40 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Figure 3. ST90E40 Block Diagram



GENERAL DESCRIPTION (Continued)

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other systemmsiming functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

1.2 PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST9040 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$/V_{PP}. *Reset (input, active low) or V_{PP} (input).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input VPP.

iNT0, INT7. External interrupts (input, active on rising or falling edge). External interrupt inputs 0 and 7 respectively. INT0 channel may also be used for the timer watchdog interrupt.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter. *Must be tied to V_{SS}.*

V_{DD}. Main Power Supply Voltage (5V ± 10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 56 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as alternate functions.

1.2.1 I/O PORT ALTERNATE FUNCTIONS

Each pin of the I/O ports of the ST90E40/T30 may assume software programmable Alternative Functions as shown in the Pin Configuration Tables. Due to Bonding options for the packages, some functions may not be present, Table 4 shows the Functions allocated to each I/O Port pin and a summary of packages for which they are available.

PIN DESCRIPTION (Continued)

Table 4. ST90E40, T40 I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
Port. bit				PLCC	PQFP	PSDIP
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24	39	32
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25	40	33
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26	41	34
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27	42	35
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28	43	36
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29	44	37
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30	45	38
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31	46	39
P1.0	A8	O	Address bit 8	23	38	31
P1.1	A9	O	Address bit 9	22	37	30
P1.2	A10	O	Address bit 10	21	36	29
P1.3	A11	O	Address bit 11	20	35	28
P1.4	A12	O	Address bit 12	19	34	
P1.5	A13	O	Address bit 13	18	33	
P1.6	A14	O	Address bit 14	17	31	
P1.7	A15	O	Address bit 15	16	30	
P2.0	NMI	I	Non-Maskable Interrupt	44	64	51
P2.0	ROMless	I	ROMless Select (Mask option)	44	64	51
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45	65	NC
P2.1	SDI	I	SPI Serial Data Out	45	65	52
P2.2	INT2	I	External Interrupt 2	46	66	53
P2.2	SCK	O	SPI Serial Clock	46	66	53
P2.3	SDO	O	SPI Serial Data In	47	67	54
P2.4	INT1	I	External Interrupt 1	48	68	
P2.4	$\overline{WRSTB5}$	I	Handshake Write Strobe P5	48	68	
P2.5	WRRDY5	O	Handshake Write Ready P5	49	69	
P2.6	INT3	I	External Interrupt 3	50	70	
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50	70	
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50	70	
P2.7	RDRDY5	O	Handshake Read Ready P5	51	71	
P3.0	T0INA	I	MF Timer 0 Input A	15	29	27
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15	29	27
P3.1	T0OUTA	O	MF Timer 0 Output A	14	28	26
P3.2	T0INB	I	MF Timer 0 Input B	13	27	25
P3.3	T0OUTB	O	MF Timer 0 Output B	12	26	24
P3.4	T1INA	I	MF Timer 1 Input A	11	25	23

PIN DESCRIPTION (Continued)

Table 4. ST90E40, T40 I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment		
Port. bit				PLCC	PQFP	PSDIP
P3.5	T1OUTA	O	MF Timer 1 Output A	10	24	22
P3.6	T1INB	I	MF Timer 1 Input B	9	23	20
P3.7	T1OUTB	O	MF Timer 1 Output B	8	22	19
P4.0	Ain0	I	A/D Analog Input 0	52	72	55
P4.1	Ain1	I	A/D Analog Input 1	53	73	56
P4.2	Ain2	I	A/D Analog Input 2	54	74	1
P4.3	Ain3	I	A/D Analog Input 3	55	75	2
P4.4	Ain4	I	A/D Analog Input 4	61	4	8
P4.5	Ain5	I	A/D Analog Input 5	56	76	3
P4.6	Ain6	I	A/D Analog Input 6	57	77	4
P4.7	Ain7	I	A/D Analog Input 7	58	78	5
P5.0		I/O	I/O Handshake Port 5	3	15	
P5.1		I/O	I/O Handshake Port 5	2	14	
P5.2		I/O	I/O Handshake Port 5	1	13	14
P5.3		I/O	I/O Handshake Port 5	68	11	13
P5.4		I/O	I/O Handshake Port 5	65	8	12
P5.5		I/O	I/O Handshake Port 5	64	7	11
P5.6		I/O	I/O Handshake Port 5	63	6	10
P5.7		I/O	I/O Handshake Port 5	62	5	9
P7.0	SIN	I	SCI Serial Input	43	61	50
P7.1	SOUT	O	SCI Serial Output	42	60	49
P7.1	ROMless	I	ROMless Select (Mask option)	42	60	49
P7.2	INT4	I	External Interrupt 4	41	59	48
P7.2	TXCLK	I	SCI Transmit Clock Input	41	59	48
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41	59	48
P7.3	INT5	I	External Interrupt 5	40	58	47
P7.3	RXCLK	I	SCI Receive Clock Input	40	58	47
P7.3	ADTRG	I	A/D Conversion Trigger	40	58	47
P7.4	INT6	I	External Interrupt 6	39	57	
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39	57	
P7.5	$\overline{WAIT}$	I	External Wait Input	38	56	
P7.6	WDOUT	O	T/WD Output	37	55	46
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37	55	46
P7.7	WDIN	I	T/WD Input	36	54	45
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36	54	45

1.1 MEMORY

The memory of the ST90E40 is functionally divided into two areas, the Register File and Memory. The Memory is divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E40 16K bytes of on-chip EPROM memory are selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space, while the ST90T40 OTP version has the top 64 bytes of the EPROM reserved by SGS-THOMSON for testing purposes. The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of on-chip RAM memory at memory addresses 200h through 2FFh.

WARNING. *The ST90T40 has its 64 upper bytes in the internal EPROM reserved for testing purpose.*

External memory may be addressed using the multiplexed address and data buses (Alternate Functions of Ports 0 and 1). At addresses greater than the first 16K of program space, the ST90E40 executes external memory cycles for instruction fetches. Additional Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may also be used as RAM memory for minimum chip count systems.

1.2 EPROM PROGRAMMING

The 16384 bytes of EPROM memory of the ST90E40 (16320 for the ST90T40) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

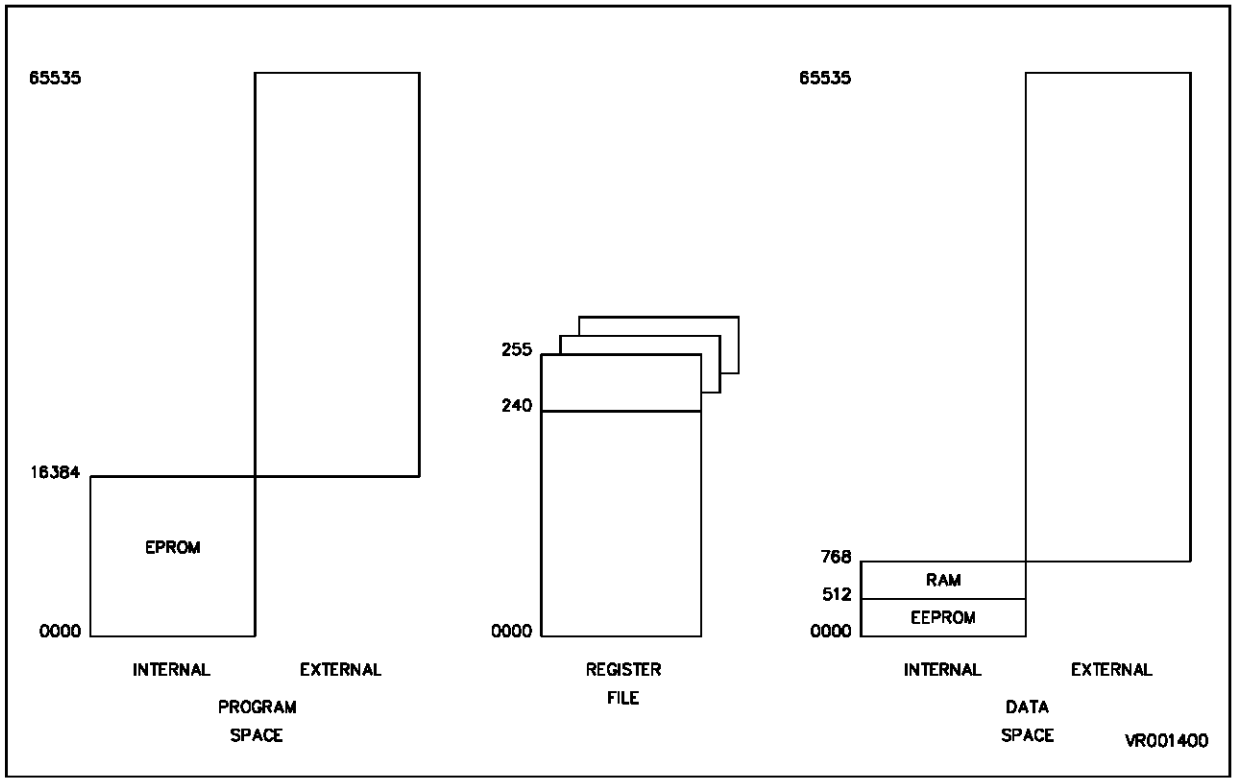
1.2.1 Eprom Erasing

The EPROM of the windowed package of the ST90E40 may be erased by exposure to Ultra-Violet light.

The erasure characteristic of the ST90E40 is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlight and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST90E40 packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

The recommended erasure procedure of the EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537Å. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST90E40 should be placed within 2.5cm (1Inch) of the lamp tubes during erasure.

Figure 4. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} = AV_{SS} < AV_{DD} \leq V_{DD}$	V
V_I	Input Voltage	– 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	– 0.3 to V_{DD} +0.3	V
V_{PP}	Input Voltage on V_{PP} Pin	-0.3 to 13.5	V
T_{STG}	Storage Temperature	– 55 to + 150	°C
I_{INJ}	Pin Injection Current Digital	-5 to 5	mA
I_{INJ}	Pin Injection Current Analog	-5 to 5	mA
	Maximum accumulated pin injection Current in the device	-50 to 50	mA

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. All voltages are referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Clock Frequency (INTCLK)		12	MHz

DC ELECTRICAL CHARACTERISTICS

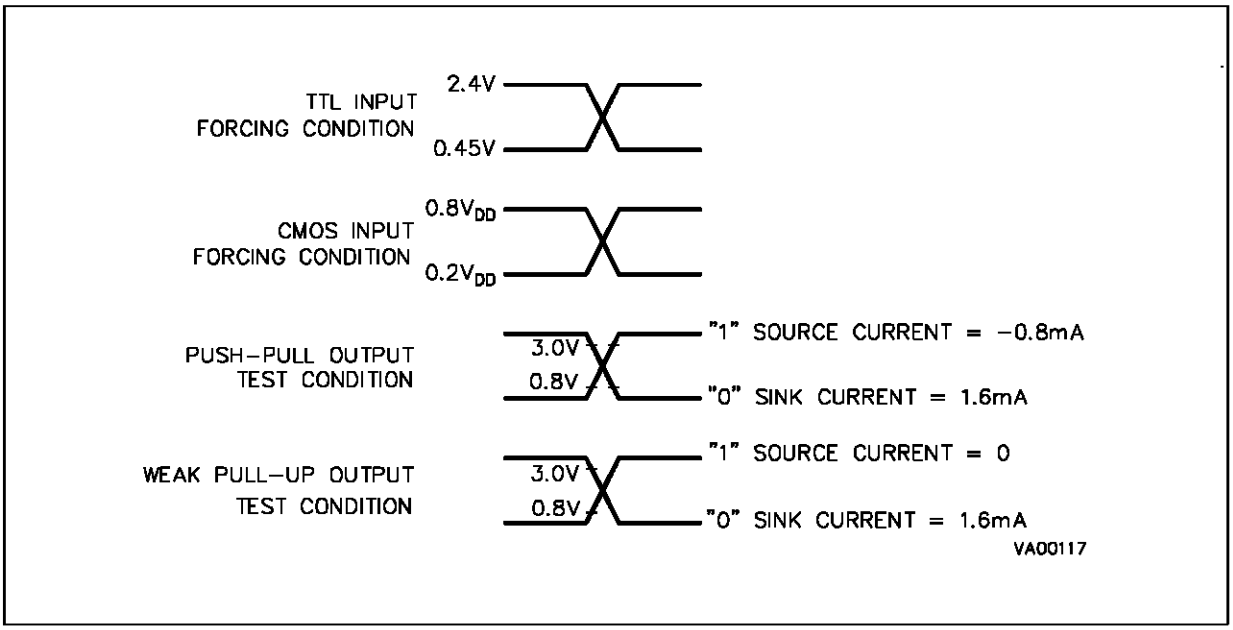
V$_{DD}$ = 5V ± 10% T_A = – 40°C to + 85°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	$\overline{\text{RESET}}$ Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	$\overline{\text{RESET}}$ Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	$\overline{\text{RESET}}$ Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = 1.6mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 50	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V, under Reset	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{LKRS}	$\overline{\text{Reset}}$ Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	– 3		+3	µA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
V_{PP}	EPROM Programming Voltage		12.2	12.5	12.8	V
I_{PP}	EPROM Programming Current				30	mA

DC TEST CONDITIONS



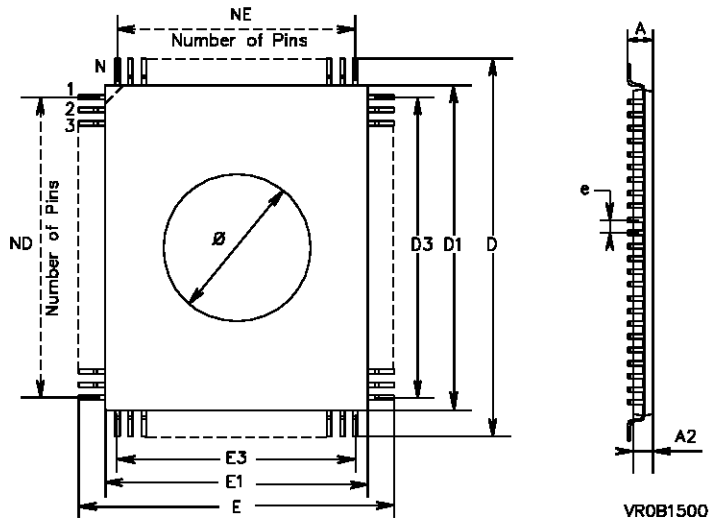
AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40°C to + 85°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{DD}	Run Mode Current no CPUCLK prescale, Clock divide by 2	24MHz			50	mA
I_{DP2}	Run Mode Current Prescale by 2 Clock divide by 2	24MHz			30	mA
I_{WFI}	WFI Mode Current no CPUCLK prescale, Clock divide by 2	24MHz			20	mA
I_{HALT}	HALT Mode Current	24MHz		50	100	µA

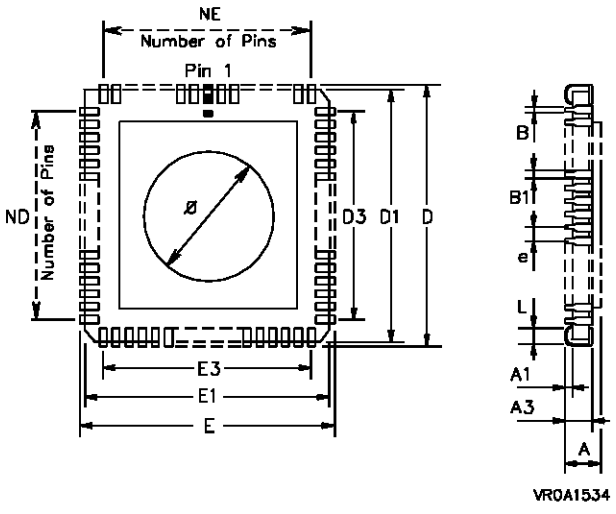
PACKAGE MECHANICAL DATA

80-Pin Ceramic Quad Flat Package with Window



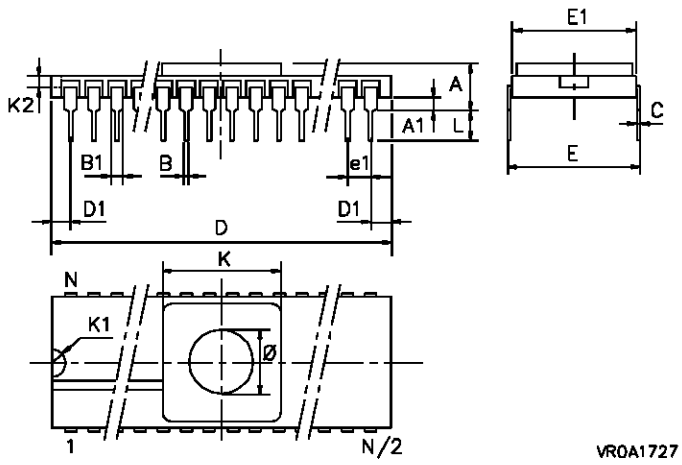
Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A		3.55			0.14	
A2		3.40			0.133	
D		23.90			0.941	
D1		20.00			0.787	
D3		18.40			0.724	
E		17.90			0.705	
E1		14.00			0.551	
E3		12.00			0.472	
Ø		7.62			0.3	
e		0.80			0.032	
Number of Pins						
N	80					
ND	24					
NE	16					

68-Pin Ceramic Leadless Chip Carrier with Window



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A		4.47			0.176	
A1		0.89			0.035	
A3		-			-	
B		0.48			0.019	
B1		-			-	
D		25.1			0.990	
D1		23.6			0.930	
D3		20.3			0.800	
E		25.1			0.990	
E1		23.6			0.930	
E3		20.3			0.800	
Ø		8			0.32	
e		1.27			0.050	
Number of Pins						
N	68					
ND	16					
NE	16					

56-Pin Ceramic Shrink Dual-In-line Package with window, 600 Mil Width



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
A1						
B						
B1						
C						
D						
D1						
E	–	–	–	–	–	–
E1						
L						
e1						
Ø						
	Number of Pins					
N	56					

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90E40L1/ES(1)	24MHz	0°C to + 70°C	CLCC68W
ST90E40G1/ES(1)		0°C to + 70°C	CQFP80W
ST90E40D1/ES(1)		0°C to + 70°C	CSDIP56W
ST90T40C6	24MHz	-40°C to + 85°C	PLCC68
ST90T40Q1		0°C to + 70°C	PQFP80
ST90T40B6		-40°C to + 85°C	PSDIP56

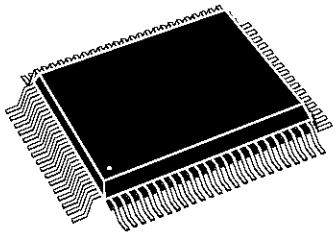
Note . EPROM parts are tested at 25°C only

SGS-THOMSON MICROELECTRONICS

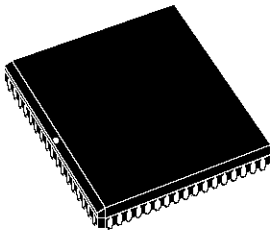
ST90R40

ROMLESS HCMOS MCU WITH EEPROM, RAM AND A/D CONVERTER

- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time:500ns (12MHz internal)
- ROMless to allow maximum external memory flexibility
- Internal Memory :
  RAM 256 bytes
  EEPROM 512 bytes
  224 general purpose registers available as RAM, accumulators or index pointers (register file)
- 80-pin Plastic Quad Flat Pack Package for ST90R40Q
- 68-lead Plastic Leaded Chip Carrier package for ST90R40C
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 40 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile development tools, including assembler, linker, C-compiler, archiver, graphic orinted debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9040 16K ROM device (also available in windowed and One Time Programmable EPROM packages)



PQFP80



PLCC68

(Ordering Information at the end of the Datasheet)

Figure 1. 80 Pin PQFP Package

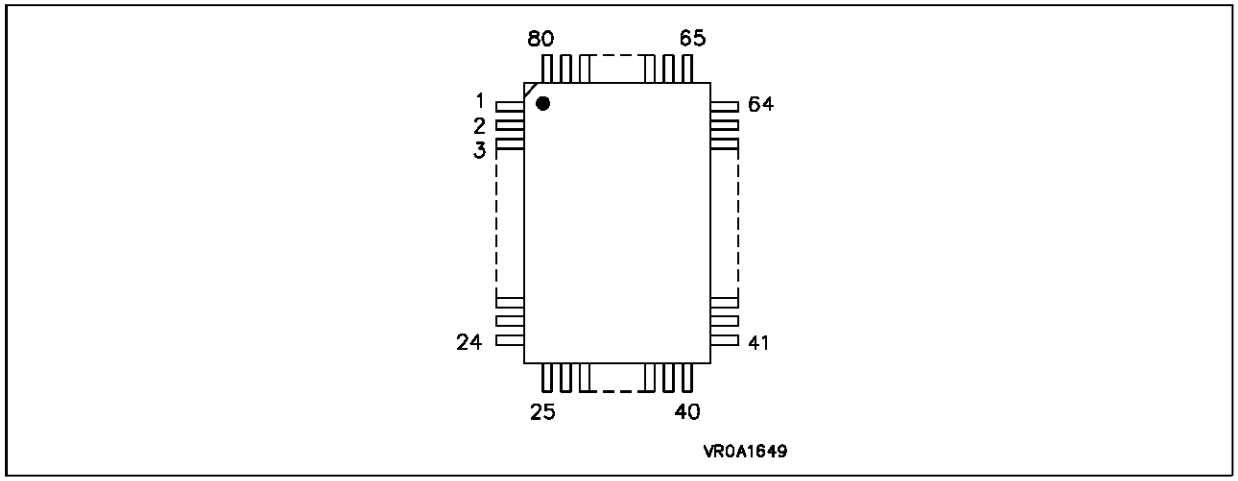


Table 1. ST90R40Q Pin Description

Pin	Name
1	AV_{SS}
2	AV_{SS}
3	NC
4	P44/AIN4
5	P57
6	P56
7	P55
8	P54
9	INT7
10	INT0
11	P53
12	NC
13	P52
14	P51
15	P50
16	OSCOUT
17	V_{SS}
18	V_{SS}
19	NC
20	OSCIN
21	$\overline{RESET}$
22	P37/T1OUTB
23	P36/T1INB
24	P35/T1OUTA

Pin	Name
25	P34/T1INA
26	P33/T0OUTB
27	P32/T0INB
28	P31/T0OUTA
29	P30/P/$\overline{D}$/T0INA
30	A15
31	A14
32	NC
33	A13
34	A12
35	A11
36	A10
37	A9
38	A8
39	A0/D0
40	A1/D1

Pin	Name
64	P20/NMI
63	NC
62	V_{SS}
61	P70/SIN
60	P71/SOUT
59	P72/INT4/TXCLK /CLKOUT
58	P73/INT5 /RXCLK/ADTRG
57	P74/P/$\overline{D}$/INT6
56	P75/$\overline{WAIT}$
55	P76/WDOUT /$\overline{BUSREQ}$
54	P77/WDIN /$\overline{BUSACK}$
53	R/$\overline{W}$
52	NC
51	$\overline{DS}$
50	$\overline{AS}$
49	NC
48	V_{DD}
47	V_{DD}
46	A7/D7
45	A6/D6
44	A5/D5
43	A4/D4
42	A3/D3
41	A2/D2

Pin	Name
80	AV_{DD}
79	NC
78	P47/AIN7
77	P46/AIN6
76	P45/AIN5
75	P43/AIN3
74	P42/AIN2
73	P41/AIN1
72	P40/AIN0
71	P27/RRDY5
70	P26/INT3 /$\overline{RDSTB5}$/P/$\overline{D}$
69	P25/WRRDY5
68	P24/INT1 /$\overline{WRSTB5}$
67	P23/SDO
66	P22/INT2/SCK
65	P21/SDI/P/$\overline{D}$

Figure 2. 68 Pin PLCC Package

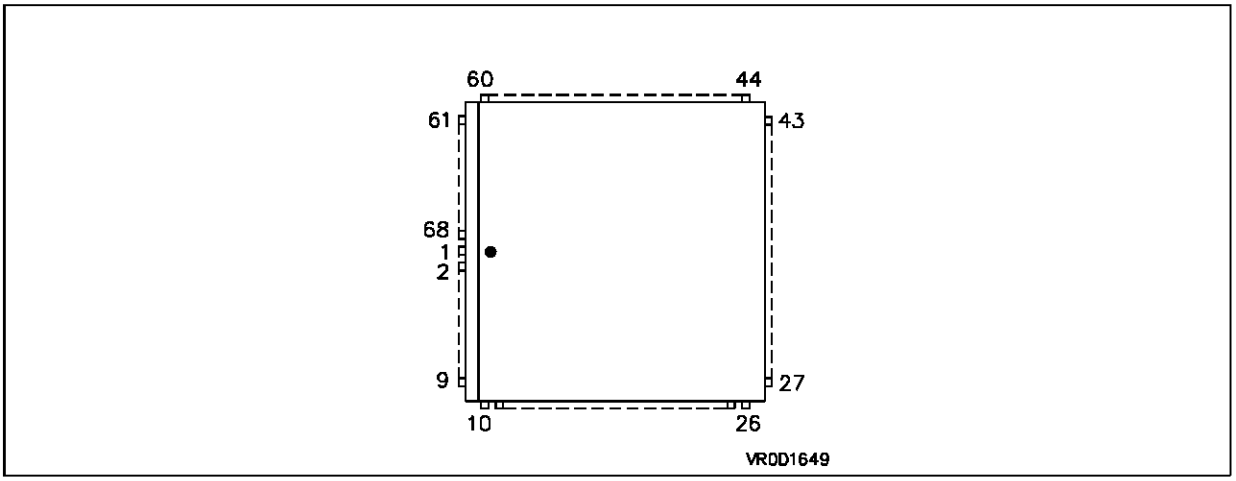


Table 2. ST90R40C Pin Description

Pin	Name
61	P44/Ain4
62	P57
63	P56
64	P55
65	P54
66	INT7
67	INT0
68	P53
● 1	P52
2	P51
3	P50
4	OSCOUT
5	V_{SS}
6	OSCIN
7	$\overline{\text{RESET}}$
8	P37/T1OUTB
9	P36/T1INB

Pin	Name
10	P35/T1OUTA
11	P34/T1INA
12	P33/T0OUTB
13	P32/T0INB
14	P31/T0OUTA
15	P30/P/$\overline{D}$/T0INA
16	A15
17	A14
18	A13
19	A12
20	A11
21	A10
22	A9
23	A8
24	A0/D0
25	A1/D1
26	A2/D2

Pin	Name
43	P70/SIN
42	P71/SOUT
41	P72/CLKOUT /TXCLK/INT4
40	P73/ADTRG /RXCLK/INT5
39	P74/P/$\overline{D}$/INT6
38	$\overline{\text{P75/WAIT}}$
37	P76/WDOUT /$\overline{\text{BUSREQ}}$
36	P77/WDIN /$\overline{\text{BUSACK}}$
35	R/W
34	$\overline{\text{DS}}$
33	$\overline{\text{AS}}$
32	V_{DD}
31	A7/D7
30	A6/D6
29	A5/D5
28	A4/D4
27	A3/D3

Pin	Name
60	AV_{SS}
59	AV_{DD}
58	P47/Ain7
57	P46/Ain6
56	P45/Ain5
55	P43/Ain3
54	P42/Ain2
53	P41/Ain1
52	P40/Ain0
51	P27/RRDY5
50	P26/$\overline{\text{INT3}}$ /$\overline{\text{RDSTB}}$5/P/$\overline{D}$
49	P25/WRRDY5
48	P24/$\overline{\text{INT1}}$ /$\overline{\text{WRSTB}}$5
47	P23/SDO
46	P22/INT2/SCK
45	P21/SDI/P/$\overline{D}$
44	P20/NMI

1.1 GENERAL DESCRIPTION

The ST90R40 is a ROMLESS member of the ST9 family of microcontrollers, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The ROMLESS part may be used for the prototyping and pre-production phases of development, and offers the maximum in program flexibility in production systems.

The ST90R40 is fully compatible with the ST9040 ROM version and this datasheet will thus provide only information specific to the ROMLESS device.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9040 ROM-BASED DEVICE.

The ROMLESS ST90R40 can be configured as a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

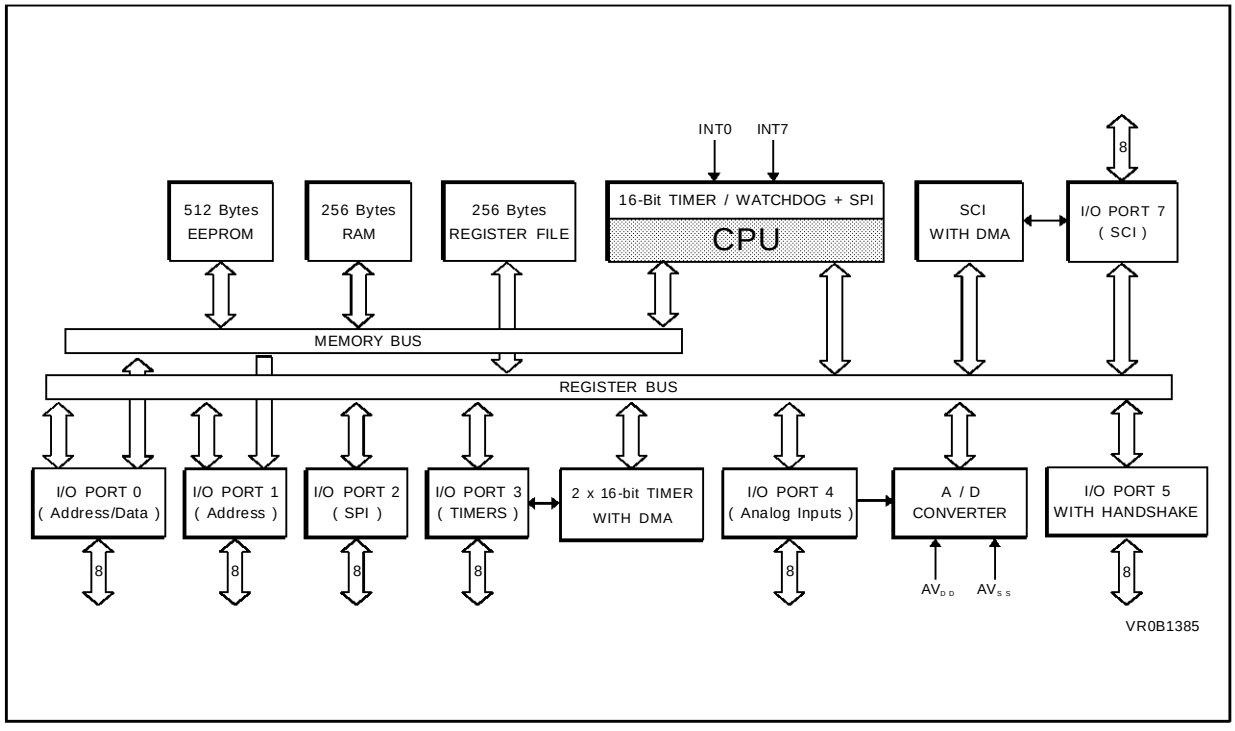
The nucleus of the ST90R40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-BUS, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90R40 with up to 56 I/O lines dedicated to memory addressing or digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing and status signals, address lines, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three memory spaces are available: Program Memory (external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

Figure 3. Block Diagram



GENERAL DESCRIPTION (Continued)

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

1.2 PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90R40 accesses on-chip Data memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for memory transactions. R/$\overline{W}$ is low when writing to program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$. *Reset (input, active low).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter. *Must be tied to V_{SS}.*

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

AD0-AD7, (P0.0-P0.7) *Address/Data Lines (Input/Output, TTL or CMOS compatible).* 8 lines providing a multiplexed address and data bus, under control of the $\overline{AS}$ and $\overline{DS}$ timing signals.

A8-A15 *Address Lines (Output, TTL or CMOS compatible).* 8 lines providing non-multiplexing address bus, under control of the $\overline{AS}$ and $\overline{DS}$ timing signals.

P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 40 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

1.2.1 I/O PORT ALTERNATE FUNCTIONS

Each pin of the I/O ports of the ST90R40 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 3 shows the Functions allocated to each I/O Port pins.

PIN DESCRIPTION (Continued)

Table 3. I/O Port Alternate Function Summary

I/O PORT	Name	Function IN/OUT	Alternate Function	Pin Assignment	
Port.bit				PQFP80	PLCC68
P0.0	A0/D0	I/O	Address/Data bit 0 mux	39	24
P0.1	A1/D1	I/O	Address/Data bit 1 mux	40	25
P0.2	A2/D2	I/O	Address/Data bit 2 mux	41	26
P0.3	A3/D3	I/O	Address/Data bit 3 mux	42	27
P0.4	A4/D4	I/O	Address/Data bit 4 mux	43	28
P0.5	A5/D5	I/O	Address/Data bit 5 mux	44	29
P0.6	A6/D6	I/O	Address/Data bit 6 mux	45	30
P0.7	A7/D7	I/O	Address/Data bit 7 mux	46	31
P1.0	A8	O	Address bit 8	38	23
P1.1	A9	O	Address bit 9	37	22
P1.2	A10	O	Address bit 10	36	21
P1.3	A11	O	Address bit 11	35	20
P1.4	A12	O	Address bit 12	34	19
P1.5	A13	O	Address bit 13	33	18
P1.6	A14	O	Address bit 14	31	17
P1.7	A15	O	Address bit 15	30	16
P2.0	NMI	I	Non-Maskable Interrupt	64	44
P2.1	P/$\overline{D}$	O	Program/Data Space Select	65	45
P2.1	SDI	I	SPI Serial Data Out	65	45
P2.2	INT2	I	External Interrupt 2	66	46
P2.2	SCK	O	SPI Serial Clock	66	46
P2.3	SDO	O	SPI Serial Data In	67	47
P2.4	INT1	I	External Interrupt 1	68	48
P2.4	$\overline{WRSTB5}$	O	Handshake Write Strobe P5	68	48
P2.5	WRRDY5	I	Handshake Write Ready P5	69	49
P2.6	INT3	I	External Interrupt 3	70	50
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	70	50
P2.6	P/$\overline{D}$	O	Program/Data Space Select	70	50
P2.7	RDRDY5	O	Handshake Read Ready P5	71	51
P3.0	T0INA	I	MF Timer 0 Input A	29	15
P3.0	P/$\overline{D}$	O	Program/Data Space Select	29	15
P3.1	T0OUTA	O	MF Timer 0 Output A	28	14
P3.2	T0INB	I	MF Timer 0 Input B	27	13
P3.3	T0OUTB	O	MF Timer 0 Output B	26	12
P3.4	T1INA	I	MF Timer 1 Input A	25	11

PIN DESCRIPTION (Continued)

Table 3. I/O Port Alternate Function Summary (Continued)

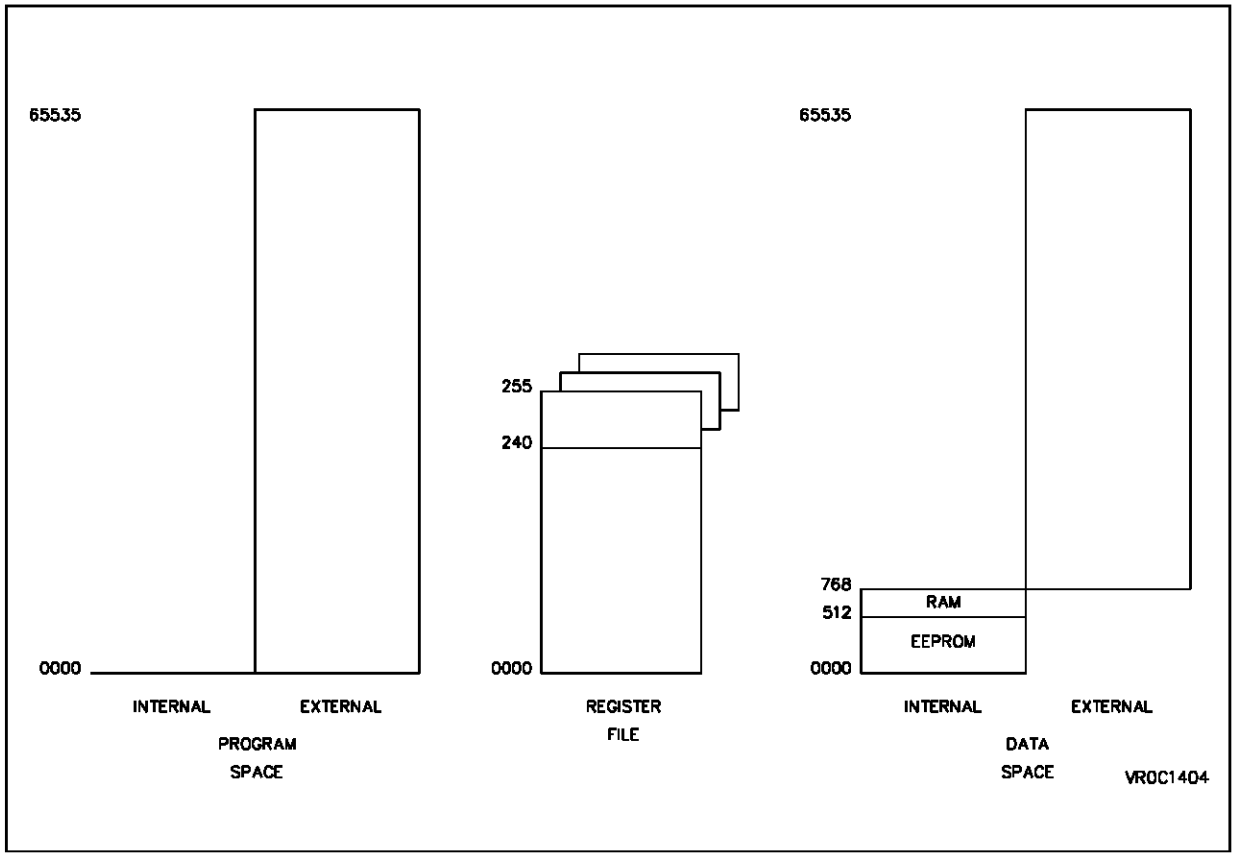
I/O PORT	Name	Function IN/OUT	Alternate Function	Pin Assignment	
Port.bit				PQFP80	PLCC68
P3.5	T1OUTA	O	MF Timer 1 Output A	24	10
P3.6	T1INB	I	MF Timer 1 Input B	23	9
P3.7	T1OUTB	O	MF Timer 1 Output B	22	8
P4.0	Ain0	I	A/D Analog Input 0	72	52
P4.1	Ain1	I	A/D Analog Input 1	73	53
P4.2	Ain2	I	A/D Analog Input 2	74	54
P4.3	Ain3	I	A/D Analog Input 3	75	55
P4.4	Ain4	I	A/D Analog Input 4	4	61
P4.5	Ain5	I	A/D Analog Input 5	76	56
P4.6	Ain6	I	A/D Analog Input 6	77	57
P4.7	Ain7	I	A/D Analog Input 7	78	58
P5.0		I/O	I/O Handshake Port 5	15	3
P5.1		I/O	I/O Handshake Port 5	14	2
P5.2		I/O	I/O Handshake Port 5	13	1
P5.3		I/O	I/O Handshake Port 5	11	68
P5.4		I/O	I/O Handshake Port 5	8	65
P5.5		I/O	I/O Handshake Port 5	7	64
P5.6		I/O	I/O Handshake Port 5	6	63
P5.7		I/O	I/O Handshake Port 5	5	62
P7.0	SIN	I	SCI Serial Input	61	43
P7.1	SOUT	O	SCI Serial Output	60	42
P7.2	INT4	I	External Interrupt 4	59	41
P7.2	TXCLK	I	SCI Transmit Clock Input	59	41
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	59	41
P7.3	INT5	I	External Interrupt 5	58	40
P7.3	RXCLK	I	SCI Receive Clock Input	58	40
P7.3	ADTRG	I	A/D Conversion Trigger	58	40
P7.4	INT6	I	External Interrupt 6	57	39
P7.4	P/$\overline{D}$	O	Program/Data Space Select	57	39
P7.5	$\overline{WAIT}$	I	External Wait Input	56	38
P7.6	WDOUT	O	T/WD Output	55	37
P7.6	$\overline{BUSREQ}$	I	External Bus Request	55	37
P7.7	WDIN	I	T/WD Input	54	36
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	54	36

1.3 MEMORY

The memory of the ST90R40 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90R40 addresses all program memory in the external PROGRAM space. The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of on-chip RAM memory at addresses 200h through 2FFh.

The External Memory spaces are addressed using the multiplexed address and data buses on Ports 0 and 1. Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may be used as RAM memory.

Figure 4. Memory Spaces



ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90R40C6	24MHz	-40°C to + 85°C	PLCC68
ST90R40Q1		0 °C to + 70 °C	PQFP80